MULTIWAY SPEAKER SYSTEMS WITH WAVE DIGITAL BRANCHING FILTER BANK

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***Abstract* – This paper describes a digital modulator for a class-D power audio amplifier using the oversampling and noise-shaping techniques. Results of the simulation of the output signal spectrum for the interesting frequency band of a sinusoidal input signal are shown. Such modulator achieves a signal-to-noise ratio (SNR) near to 88dB. The concept for an analogue compensating circuit for suppressing the power supply ripple is also presented.**

I. INTRODUCTION

The physics of sound reproduction makes it quite difficult for a single speaker to handle the whole audio-frequency range. Therefore, for high fidelity applications, most speaker systems consist of multiple speakers, each of them reproducing a specific band of the overall audio-frequency range. In typical realizations, this range is divided into two or three bands.

Using CD players, R-DAT, Sony mini discs, digital audio processors, digital TV, digital broadcasting systems, and so on, we have a direct access to the digital signal sources. Therefore it is reasonable to supply digital signal directly to the speaker. This idea, which is based on the concept of a digital modulator driving the class-D power audio amplifier and on the noise-shaping technique, is presented in this contribution.

II. THE DIGITAL SPEAKER SYSTEM

Block diagram of the digital speaker system is depicted in Fig. 2 [1, 2, 3]. The digital input signal (in the CD player standard, i.e. with sampling rate f_s=44.1kHz) is divided into two channels: left and right, by a digital audio interface receiver. Then it is split into two bands: a lowpass and a highpass band using a wave digital branching filter bank. Wave digital filter bank has been chosen not only for its power-complementarity but also because of other well known advantages of wave digital filters such as small sensitivity to coefficient variations, robust stability and so on [4]. The next stage is a hybrid PWM modulator. For suppression of the quantization and the modulation noises the oversampling technique together with the noise-shaping technique are implemented in the hybrid PWM modulator. The output signal from the modulator is a square wave with the duty ratio depending on the represented values. This signal controls the power pulse amplifier through a specialized analogue compensating circuit proposed in this paper. In the present version, pulse-width modulators (PWM's) connected to the pulse power amplifiers serve as D/A converters. For suppressing the power supply ripple, an analogue compensating circuit is used. Additional passive LC lowpass filter is used in order to suppress the noise and the disturbing modulation products.

Power Pulse Amplifier

Simplified diagram of a power pulse amplifier is shown in Fig. 1. The input signals G_{1H} and G_{1L} are transformed by the gate drivers and control gates of the power MOSFET transistors Q1 and Q2. The switching frequency of this circuit can be as high as ca. 1MHz [5] according to the use of the ultra low gate-charge MOSFETs and high speed gate drivers. The power pulse amplifier is supplied by two equal voltage sources V1 and V2. Speaker is connected to the inverter output through a passive LC low-pass filter in order to suppress the noise and the modulation frequency.

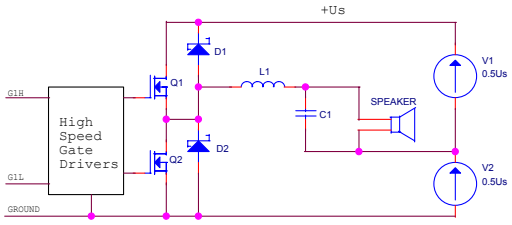

Figure 1: Simplified diagram of a power pulse amplifier

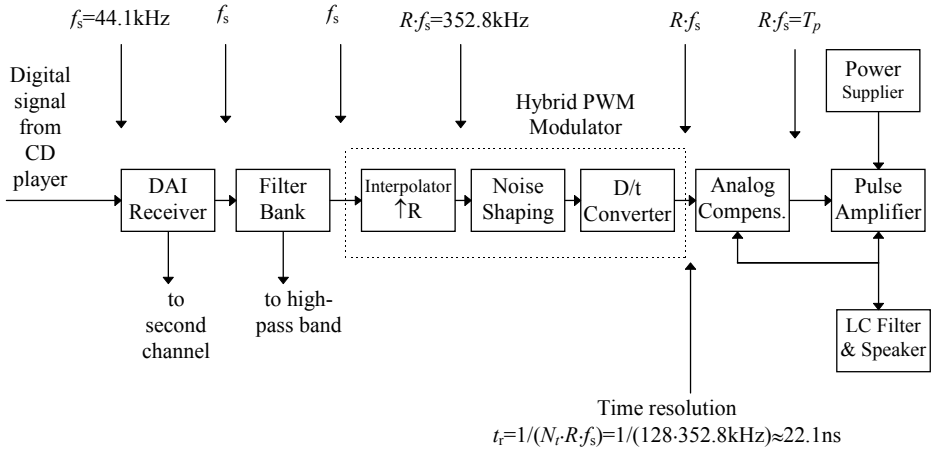

Figure 2: Block diagram for the proposed digital speaker system

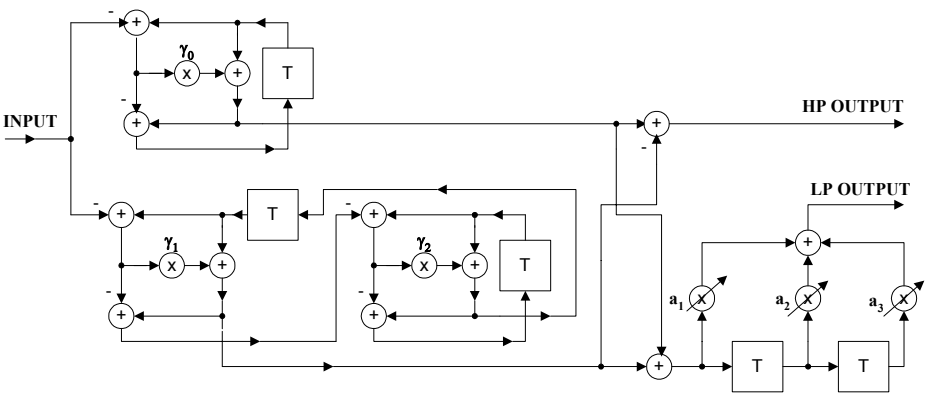

Figure 3: Block diagram for the digital branching filter bank

Wave digital branching filter bank

In a typical three way crossover system, the audio-frequency range is divided into three separate bands. In our case, we use two bands only, namely the tweeter band and the joint woofer/midrange band. In both considered active-digital crossover versions, they are realized using a wave digital branching filter bank shown in Fig. 3 [3, 4]. An additional lowpass FIR filter cascaded with the lowpass branch forms a corrected woofer/midrange band. The function of this filter can also be referred to as the midrange correction, because, by this means, we reduce the midrange-band-gain of the power-complementary wave digital branching filter bank, compensating the nonuniform frequency characteristic of two identical woofer/midrange speakers used in the experimental system.

Hybrid pulse width modulator

The idea of the modified pulse-width modulation (PWM) technique used in our system is depicted in Fig. 1. The modulator input signal (i.e., the output signal of the filter bank) is first R times interpolated; R being the oversampling ratio of this signal sampled originally with frequency f_s.=44.1kHz The idea of oversampling consists in an increase of the signal sampling rate to the value for which a low-resolution quantizer is sufficient for the signal representation with required precision. Therefore using oversampling, we can reduce requirements for D/A converter (quantizer) which otherwise should be a very precise and expensive element. In our solution [1, 2], the power pulse amplifier works as a one-bit D/A converter

In the next step, the quantization noise is shaped. The modulated signal is then converted into signals controlling the power inverter.

The chosen oversampling ratio R=8 is a compromise between the power MOSFET switching losses and the selectivity of the output passive lowpass smoothing filter. The transistor switching frequency is

$R \cdot f_s$=352.8kHz. In the next step, the quantization noise is shaped. The modulated signal is then converted into signals controlling the power pulse amplifier. The factor N_t=128 is used to guarantee the required time-resolution of the conversion of digitally-coded magnitudes to transistor switching times in the power pulse amplifier. It gives the switching frequency equal to $f_s \cdot R \cdot N_t$=45.1584MHz, and the time resolution t_r=1/45.1584MHz≈22.1ns. This value is suitable for ordinary HCMOS counters.

Digital-to-analog converters with noise shaping

Different circuit architectures can be used for spectral shaping of the quantization noise, i.e. moving it away from the band of interest 0-f_B toward higher frequencies. Block diagram of the circuit using a linear quantizer model with noise shaping is shown in Fig. 3. Output signal can be calculated as

$$Y_q(z) = X(z)H_s(z) + E_q(z)H_n(z) \ . \qquad \textbf{(1)}$$

Signal and noises transfer functions are given by equations

$$H_s(z) = \frac{H(z)}{1+H(z)} \text{ and } \quad H_n(z) = \frac{1}{1+H(z)}, \qquad \textbf{(2)}$$

respectively.

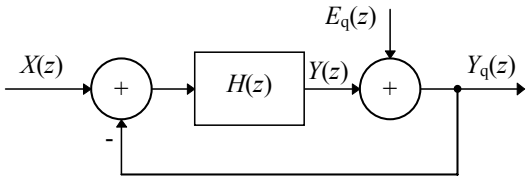

Figure 4: Block diagram circuit with noise-shaping

A properly designed circuit with noise shaping has flat frequency response $H_s(\omega)$ in the signal frequency band $0 \leq f \leq f_B$. On the other hand, $H_n(\omega)$ should have high attenuation in the frequency band $0 \leq f \leq f_B$ and a low attenuation in the band $f_B \leq f \leq f_s$. For a low oversampling ratio R, an efficient way to increase the signal-to-noise ratio is the use of a second-order loop filter.

Delta-sigma modulators (DSM's) have been used extensively in many applications as high quality ADC's and DAC's [7, 8, 10]. The linear model of the second order DSM is shown in Fig. 5. Its z-domain output can be expressed as a sum of the signal and the quantization noise components by using a linear quantiser model.

$$Y(z) = X(z)z^{-1} + (1-z^{-1})^2 E(z) \qquad \textbf{(3)}$$

Note that the input signal appears at the output through a single delay, corresponding to an all-pass function. The NTF is the expression that shapes the noise spectrum $E(z)$. The noise transfer function of the second order delta-sigma modulator is depicted in Fig. 6. For an oversampling ratio R=8 DSM, the achieved noise suppression factor is near 23dB.

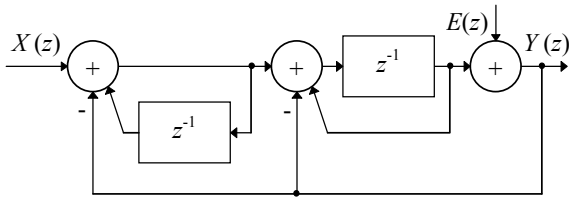

Figure 5: Linear model of the second-order delta-sigma modulator

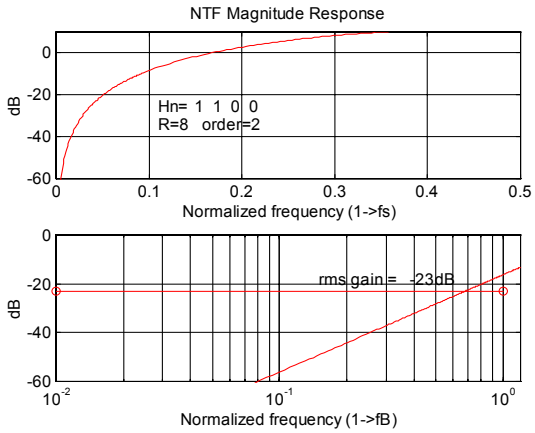

Figure 6: The noise transfer function of the second order delta-sigma modulator for R=8

Digital to time converter with noise shaping

Idea for a D/A converter [1, 2] with the D/A conversion error compensation can be combined with the idea of the PWM D/A converter based on the second order DSM as depicted in Fig. 7. The input signal $X(z)$ is transformed into signals G_{1H} and G_{1L} controlling the power inverter MOSFET transistors. High levels of these signals switch on the respective transistors. When signal G_{1H} is in the high sate, the period t_{1H} is calculated using (4) and period t_{1L} is calculated using a similar equation for signal G_{1L} in the high state.

$$t_{1H} = \begin{cases} t_{1H} = 0 & \text{for } Y(z) < 0 \\ & \text{or } k_c Y(z) < t_{ON\,min} \\ t_{1H} = t_{ONmax} & \text{for } k_c Y(z) > t_{ON\,max} \\ t_{1H} = \text{int}\left(k_c Y(z)\right) & \text{for } Y(z) > 0 \\ & \text{and } k_c Y(z) > t_{ON\,min} \\ & \text{and } k_c Y(z) < t_{ON\,max} \end{cases} \qquad \textbf{(4)}$$

where:

k_c - is an auxiliary coefficient,

t_{ON} - MOSFET transistor switch on time.

The simulated output spectrum for the interesting signal band for a sinusoidal input signal with $2/3f_B$ frequency is shown in Fig. 8. This converter achieves the signal-to-noise ratio (SNR) near to 88dB.

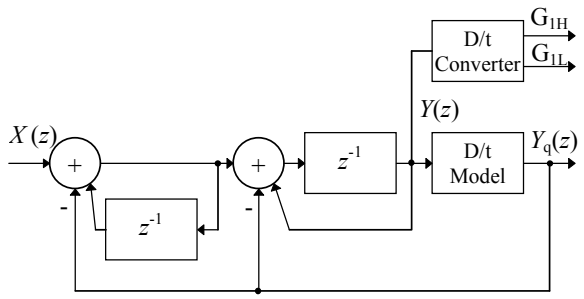

Figure 7: Block diagram of PWM D/A

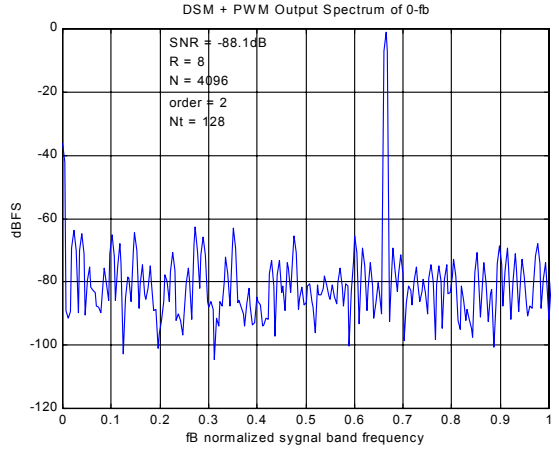

Figure 8: Output spectrum of hybrid PWM based on DSM

Analog Compensation Circuit

Simplified model of the power pulse amplifier switch (transistor) [6] is shown in Fig. 7. The transfer function is described by equation

$$y = D_{in}x \qquad \textbf{(5)}$$

where:

x - represents the supply voltage,
y - represents the output voltage,
D_{in} - is the input duty ratio.

The supply voltage ripple is transformed to the output signal. For high quality applications, a high performance supplier or a special ripple compensation circuit are needed.

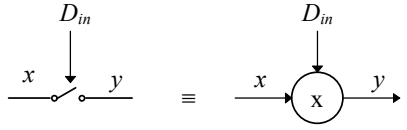

Figure 9: Simplified model of inverter switch

A solution of such a compensation circuit for the continuous time input signal can be a one-cycle control circuit [9]. A simplified diagram of such a circuit is shown in Fig. 10. The duty-ratio of a switch is controlled in such a way that in each cycle the average value of the switched variable of the switching circuit is exactly equal or proportional to the control reference in the steady state and in the transient state. One-cycle control precisely follows the control reference in one switching cycle. This guarantees that a wide bandwidth can be achieved. One-cycle control effectively rejects the power source ripple and processes power and signal in one stage, therefore, no precision dc power source is necessary. As a matter of fact, a rectified but unregulated power source with small capacitor can be used as the dc power source. One-cycle control automatically corrects the power switch transient error and the conduction error. As a result, no switching component matching is necessary. The output has no cross-over distortion. High linearity is achievable.

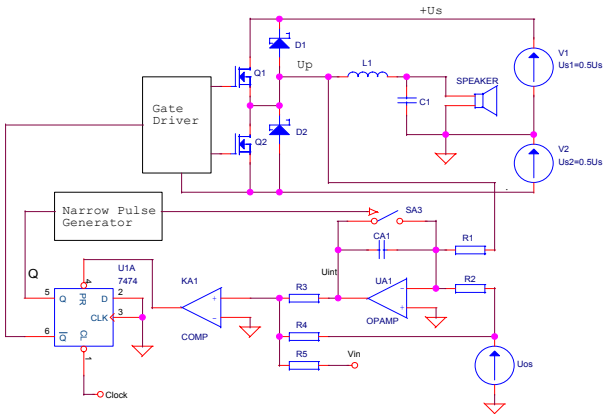

Figure 10: Simplified diagram of a one-cycle controller

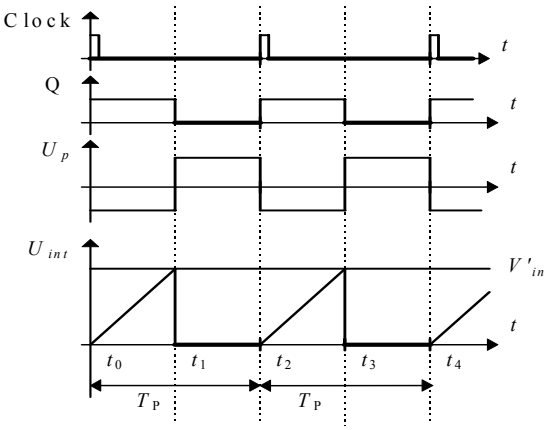

Figure 11: Waveforms of a one-cycle controller

The control function of one-cycle controller is calculated by equation

$$\int_{t_1}^{t_2}\left(\frac{u_p}{R_1 C_{A1}}-\frac{u_{os}}{R_2 C_{A1}}\right)\mathrm{d}t = v'_{in} \qquad (6)$$

and the local average of u_p is proportional to the input signal v_{in}

$$\bar{u}_p \equiv \frac{1}{T_p}\int_0^{T_p} u_p \mathrm{d}t = k v_{in} \qquad (7)$$

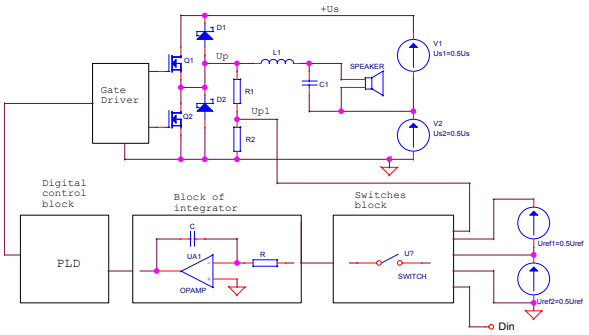

Figure 12: Diagram of analogue compensation circuit

The continuous-time signal used by a one-cycle controller is not convenient for a digital signal source. For this purpose an analogue compensation circuit is proposed by the authors. Simplified diagram fo this compensation circuit is shown in Fig. 12. Input signal is a square wave with duty ratio D_{in} and the output signal is a square wave with duty ratio D_{out}. For all components constant during the switching period T_p, it is possible to calculate D_{out} from equation

$$D_{out}(n) = \frac{U_{ref2}}{U_{p1P}(n)} D_{in}(n) - \left(1 - D_{in}(n)\right)\frac{U_{ref1}}{U_{p1P}(n)} + \\ + \left(1 - D_{out}(n-1)\right)\frac{U_{p1N}(n-1)}{U_{p1P}(n)} \qquad (8)$$

where:

U_{ref1}, U_{ref2} - reference voltages,

U_{p1P} - output voltage when transistor Q_1 is switched on,

U_{p1N} - output voltage when transistor Q_2 is switched on.

A simplified small signal model of the compensation circuit and its ripple rejections for different duty ratios D_{in} are shown in Figs. 13 and 14. Its small signal transfer function is

$$y = xD\left(\frac{\tau s}{1+\tau s}\right) \qquad (9)$$

where: τ- integrator time constant.

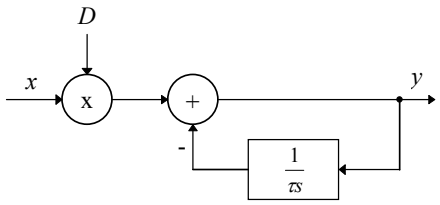

Figure 13: Small signal model of the compensation circuit

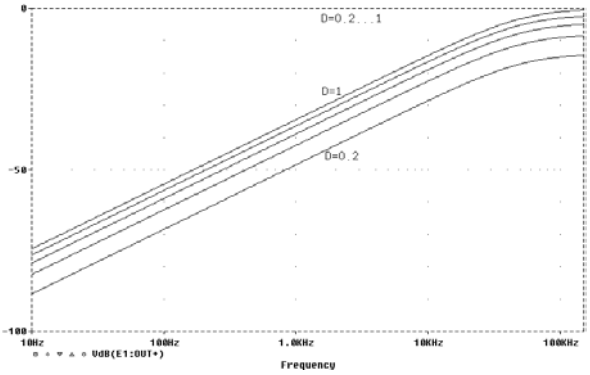

Figure 14: Compensation circuit ripple rejection

III. CONCLUSION

In the further research, the noise shaping circuit will be developed to achieve better noise rejection. In the authors' opinion, the class-D power amplifier, and especially that with the digital input, will be more popular in near future, especially for high power audio applications.

The implementation of the presented digital modulator for the class-D audio power amplifier is in the final design stage using TMS320C31 signal processor. In near future the designed digital modulator will be tested in the laboratory.

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