Adam Dąbrowski

Poznań University of Technology Institute of Electronics and Telecommunications Division for Electronic Systems and Signal Processing ul. Piotrowo 3a, 60-965 Poznań

Krzysztof Sozański

Pedagogical University of Zielona Góra Dept. of Mathematics, Physics and Technology al. Wojska Polskiego 69, 65-625 Zielona Góra

Implementation of Multirate Modified Wave Digital Filters Using Digital Signal Processors

Keywords: multirate signal processing, wave digital filters, IIR digital filters, digital signal processors

ABSTRACT

This paper describes implementation of multirate modified lattice wave digital filters using digital signal processors. A cascaded interpolators based on bireciprocal modified lattice wave digital filters for interpolating high quality audio signals are presented. The interpolators are implemented in SHARC digital signal processor (Analog Devices). The results of this implementation are presented, the frequency response of the cascaded interpolator realized by ADSP-21061 processor are shown for the interpolation ratio R=8. Such an interpolator achieves the signal-to-noise and distortion ratio S_{INAD} near to -90dB and the passband ripple $\delta_p \approx 8 \cdot 10^{-9}$ dB.

1. INTRODUCTION

According to the well known advantages of wave digital filters [4, 5] like: small passband sensitivity to coefficients, small rounding errors, big resistivity to parasitic oscillations (limit cycles), great dynamic range, low level of the rounding noise, etc. such filters are well suited for the high quality audio signal processing.



Fig. 1. Block diagrams of lattice wave digital filters (a), (b) analysis filter bank, (c) synthesis filter bank



Fig. 2. Block diagram of classical first-order all-pass section (a), (b) realization diagram of a two port adaptor

Lattice wave digital filters are built with two blocks realizing all-pass functions S_1 and S_2 . Typically blocks S_1 and S_2 are realized by a cascade of first-order and second-order all-pass sections. Wave digital filters were proposed in 70's when multiplication was a quite expensive operation. That is why they were designed with the minimum number of multipliers. A typical classical two port adaptor is depicted in Fig. 2b. It requires a single multiplier and three adders. Reflection signals b_1 and b_2 of can be calculated by equations

$$\begin{cases} b_1 = -\gamma_1 a_1 + (1 + \gamma_1) a_2 \\ b_2 = (1 - \gamma_1) a_1 + \gamma_1 a_2 \end{cases}$$
(1)

2. MODIFIED WAVE DIGITAL FILTERS

Today, modern digital signal processors (DSP's) are designed to be able to calculate one addition and one multiplication in a single operational cycle [1]. In result, the classical two port adaptor structure of Fig. 2b is ineffective in the DSP implementation, especially for the floating point arithmetics. Hence, this structure has to be changed. The idea of the so-called modified wave digital filters with equal numbers of additions and multiplications was proposed by Fettweis [3]. In Figure 3 the idea of this modification consisting in adding complementary multipliers is illustrated.



Fig. 3. Block diagram of the first-order modified all-pass section: (a) the idea of complementary multipliers, (b) realization diagram of the two port adaptor

Reflection signals b_1' and b_2' of the modified two port adaptor (Fig. 4a) can be calculated by equations



Fig. 4. Realization diagram of first-order modified all-pass section:(a), (b) case 1, (c) case 2, (d) case 3

in which coefficients γ are given by equations

$$\begin{cases} \gamma_{11} = -\gamma_1 \frac{k_{w1}}{k_{d1}} \\ \gamma_{12} = (1+\gamma_1)/k_{d1} \\ \gamma_{21} = (1-\gamma_1)k_{w1} \\ \gamma_{22} = \gamma_1 \end{cases}$$
(3)

Three cases for realizations of modified two port adaptors are possible (Fig. 4) described by equations listed in Table 1 and depicted in Figs 4b, 4c, 4d. Every realization needs four operations: two multiplications and two additions.

As an example, the realization an *N*-order branch of the lattice filter with modified first-order sections is depicted in Fig. 5. The resultant value of the branch coefficient can be calculated as

$$\gamma_s = \prod_{i=1}^{i=N} \frac{k_{di}}{k_{wi}} \quad . \tag{4}$$

Case 1 for: $\gamma_{21}=1$,	Case 2 for: $\gamma_{11}=1$,	Case 3 for: $\gamma_{11}=1$,	
<i>γ</i> ₁₂ =1	$\gamma_{12} = 1$	<i>y</i> ₂₁ =1	
$\begin{cases} k_{w1} = 1/(1-\gamma_1) \\ k_{d1} = 1+\gamma_1 \end{cases}$	$\begin{cases} k_{w1} = -(1+\gamma_1)/\gamma_1 \\ k_{d1} = 1+\gamma_1 \end{cases}$	$\begin{cases} k_{w1} = 1/(1 - \gamma_1) \\ k_{d1} = -\gamma_1/(1 - \gamma_1) \end{cases}$	
$\begin{cases} \gamma_{11} = -\gamma_1 / (1 - \gamma_1^2) \\ \gamma_{12} = 1 \\ \gamma_{21} = 1 \\ \gamma_{22} = \gamma_1 \end{cases}$	$\begin{cases} \gamma_{11} = 1\\ \gamma_{12} = 1\\ \gamma_{21} = -(1 - \gamma_1^2)/\gamma_1\\ \gamma_{22} = \gamma_1 \end{cases}$	$\begin{cases} \gamma_{11} = 1\\ \gamma_{12} = -(1 - \gamma_1^2) / \gamma_1\\ \gamma_{21} = 1\\ \gamma_{22} = \gamma_1 \end{cases}$	

Table 1 Equations for the first-order modified two port adaptor



Fig. 5. Diagram of the *N*-order branch of the lattice wave digital filter realized by first-order sections

Authors' implementation of modified first-order section using ADSP-21061digital signal processor is presented in Figure 6. To compute a single response sample, four operational cycles are necessary (with additional assumption that the program is in a cache memory[1]).



Fig. 6. Implementation of modified first-order section by ADSP-21061: (a) realization diagram of first-order section, (b) assembler realization program

3. INTERPOLATOR

A class of lattice wave digital filters referred to as bireciprocal, is suitable for the realization of interpolators. Characteristic function $K(\psi)$ of bireciprocal filters satisfies equation

$$K(\psi) = \frac{1}{K\left(\frac{1}{\psi}\right)} \quad . \tag{5}$$

For this kind of filters every even filter coefficient is equal to zero and the filter circuit is simplified. By replacing the output adder (Fig. 1c) by a switch it is possible to double the output signal sampling speed. A cascaded version of this interpolator with bireciprocal lattice modified wave digital filters is shown in Fig. 7. The filter branches are realized like in Fig. 5.



Fig. 7. Cascaded version of the interpolator for R=8

Parameters chosen by authors for the interpolator used in a class-D power audio amplifier [2] are: passband ripple $\delta_p < 0.1 dB$, oversampling ratio *R*=8, passband 4...20kHz, signal-to-noise and distortion ratio *S*_{INAD}<-90dB. Authors applied bireciprocal lattice wave elliptic digital filters for this realization. Filter coefficients are designed with authors' program prepared in Matlab environment, based on methods presented in [4, 5].

Table 2. Design parameters for interpolator stages

Stage	Order	Fp	F_{z}	$\delta_{\rm p} [{\rm dB}]$	$\delta_{\rm z}[{\rm dB}]$
1	15	0.2267	0.2733	$3.2 \cdot 10^{-9}$	90
2	7	0.1134	0.3866	1.1·10 ⁻⁹	90
3	5	0.0567	0.4433	$6 \cdot 10^{-10}$	90
Total		0.0567	0.0683	7.5·10 ⁻⁹	90



Fig. 8. Block diagram of the cascaded version of the interpolator with a single switch and resultant multipliers

The interpolator was realized with ADSP-21061 signal processor from Analog Devices using modified wave digital filters. The structure of the interpolator is depicted in Fig. 8. Resultant value of the coefficient γ_{sw1} is described by the following equation

$$\gamma_{sw1} = \gamma_{s12} \gamma_{s22} \gamma_{s32} \quad , \tag{6}$$

where: γ_{s12} , γ_{s22} , γ_{s32} are resultant coefficients of upper branches for the stages 1, 2, 3, respectively. Other resultant coefficients $\gamma_{sw2}...\gamma_{sw8}$ can be similarly calculated. Frequency response of the cascaded interpolator realized with ADSP-21061 for *R*=8 is shown in Fig. 8. The interpolator achieves the signal-to-noise and distortion ratio S_{INAD} near to -90dB and the passband ripple $\delta_{p} \approx 8 \cdot 10^{-9}$ dB. To compute the response for one input sample it needs 50 multiplications and 42 additions.



Fig. 8. Frequency response of cascaded interpolator realized by ADSP-21061 for *R*=8: (a), (c), (d) magnitude response, (b) phase response

4. CONCLUSIONS

Modified wave digital filters are very efficient for implementation by modern floating point signal processors. Especially for applications where big dynamic range of the signal is important.

REFERENCES

- [1] Analog Devices, ADSP-2106x SHARC User's Manual, Analog Devices, 1997.
- [2] Dąbrowski A., Sozański K., Multiway Speaker Systems with Wave Digital Branching Filter Bank, European Conference on Circuit Theory and Design, ECCTD'97, Budapest, Hungary, 1997.
- [3] Fettweis A. Modified Wave Digital Filters for Improved Implementation by Commercial Digital Signal Processors, Signal Processing 16, Elsever Science Publishers B.V. (North-Holland), 1989.
- [4] Fettweis A. *Wave Digital Filters: Theory and Practice*, Proceedings of the IEEE, Vol. 74, NO. 2, February 1986, pp. 270-327.
- [5] Gazsi L. *Explicit Formulas for Lattice Wave Digital Filters*, IEEE Transactions on Circuits and Systems, Vol. CAS-31, No 1, January 1985, pp. 68-88.