# Digital Control Circuit for Class-D Audio Power Amplifier

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**Abstract: This paper describes a digital speaker system with a hybrid PWM digital modulator for a class-D power audio amplifier using the oversampling and noise-shaping techniques. Results of measurements of the output signal spectrum for the audio frequency band with a sinusoidal input signal are shown. The presented speaker system achieves a signal-to-noise ratio (SNR) near to 75 dB in the audio band (20 Hz to 20 kHz).**

## I. INTRODUCTION

The physics of sound reproduction makes it very difficult for a single speaker to handle the whole audio frequency range. Therefore, for high fidelity applications, most speaker systems consist of multiple speakers, each of them reproducing a specific part of the audio band. In typical solutions, this band is divided into two or three subbands.

In most current speaker systems, a passive (typically RLC) crossover (branching filter bank) is connected between the power amplifier and the speakers (Fig. 1a). Another solution is an active crossover with a general block diagram shown in Fig. 1b. The active system is more accurate and its design is simpler.

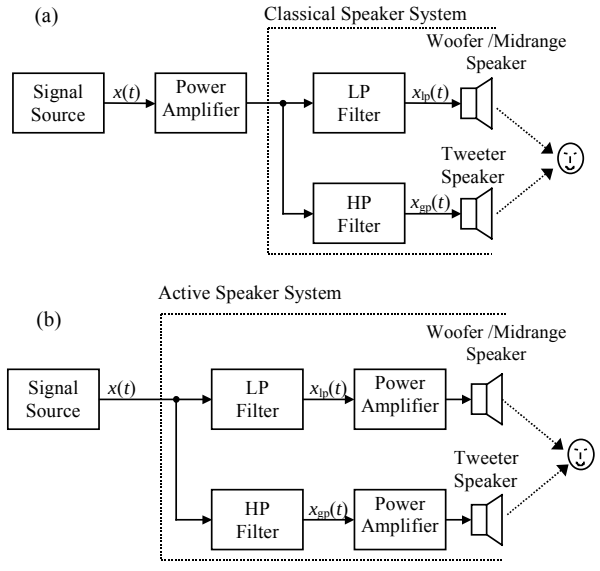


Fig. 1. Block diagrams for two alternative versions of a speaker system: (a) classical (passive) speaker system, (b) active speaker system

Using CD and DVD players, DAT, Sony mini discs, digital audio processors, digital TV, digital broadcasting systems, and so on, we have a direct access to the digital signal sources. Therefore it seems to be reasonable to supply a digital signal directly to the speaker.

A digital version of the active crossover system is proposed and discussed in this paper. It possesses many advantages over the passive realization. It should be, however, stressed that the overall system can be nowadays more expensive for the active realization because of the cost of separate power amplifiers, which are required in this case in each band as the filters should be separated from individual speakers by the power amplifiers. This will, however, change in the near future with lowering the costs of electronic components.

The presented idea of a digital speaker system is based on the concept of a digital modulator driving a class-D power audio amplifier and on the noise-shaping technique.

## II. THE DIGITAL SPEAKER SYSTEM

Block diagram of the proposed digital speaker system is depicted in Fig. 2 [11]. The digital input signal S/PDIF or AES/EBU (in the CD player standard, i.e., 16-bit with sampling rate $f_s$=44.1 kHz) is divided into two channels: left and right, by a digital audio interface receiver (DAI). Then it is split into two bands: a lowpass and a highpass band using a wave digital branching filter bank. Wave digital filter bank has been chosen not only for its power-complementarity but also because of other well known advantages of wave digital filters such as small sensitivity to coefficient variations, robust stability, etc. [5].

The next stage is a hybrid PWM modulator. For suppression of the quantization and the modulation noises the oversampling technique together with the noise-shaping technique are implemented in the hybrid PWM modulator. The modulator input signal, i.e. that at the output of the filter bank, has originally the sampling rate of $f_s$=44.1 kHz, then it is $R$ times interpolated. The chosen oversampling ratio $R$=8 only, is a compromise between the power MOSFET switching losses and the selectivity of the output passive low-pass smoothing filter. The switching frequency is then $R \cdot f_s$=352.8 kHz. In the next step, the quantization noise is shaped. The modulated signal is then converted into signals controlling the power pulse amplifier.

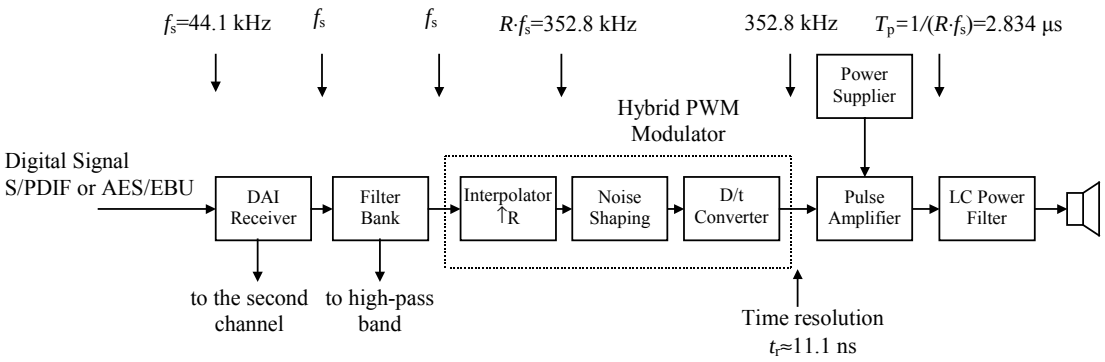


Fig. 2. Block diagram for the proposed digital speaker system

The factor $N_p$=256 is used to guarantee the required time-resolution of the conversion of digitally coded magnitudes to transistor switching times in the power pulse amplifier.

The modulator digital counter switching frequency can be calculated by equation

$$f_r = f_s R N_p \quad . \tag{1}$$

It gives the counter switching frequency equal to $f_r$=90.3168 MHz and the corresponding time resolution $t_r$=1/90.3168 MHz≈11.1 ns. This value is suitable for the ordinary HCMOS counters.

For supplying the power amplifier, a high quality power supplier with a very low ripple amplitude (<LSB) is used.

The output signal from the modulator is a square wave with the duty ratio depending on the represented values. In the present version, pulse-width modulators (PWM's) connected to the pulse power amplifiers serve as D/A converters (Fig. 3). Additional passive LC lowpass smoothing filter is connected in order to suppress the noise and the disturbing modulation products.

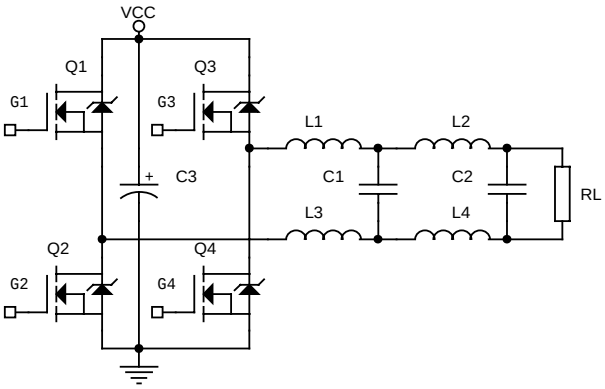


Fig. 3. Simplified diagram of a power pulse amplifier with an output smoothing filter

### A. Filter bank

In a typical three-way crossover system, the audio-frequency range is divided into three separate bands. In our case, we use two bands only, namely the tweeter band and the joint woofer/midrange band. In the considered active-digital crossover, it is realized using a modified wave digital branching filter bank shown in Fig. 4 [2, 6, 11]. Modified wave digital filters are very efficient for the implementation in modern floating point signal processors. They are especially effective for applications, in which a large dynamic signal range is important.

The filter bank was realized with ADSP-21065L signal processor (Analog Devices). To compute the response for a single input sample the program needs 8 multiplications and 8 additions [11].

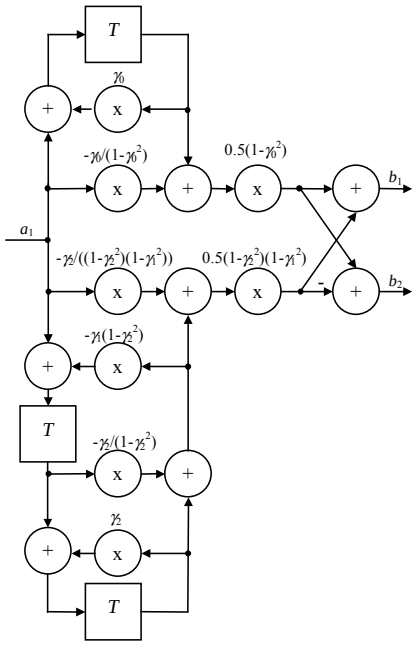


Fig. 4. Block diagram for the modified wave digital branching filter bank

*B. Hybrid Pulse Modulator*

The designed hybrid pulse modulator consists of an interpolator and a digital-to-time converter with noise shaping (Fig. 2).

*Interpolator*

Parameters chosen by the authors for the interpolator used in a class-D power audio amplifier [2, 11] are:

- passband ripple $\delta_p$<0.1 dB,
- oversampling ratio $R$=8, passband 0...20 kHz,
- signal-to-noise and distortion ratio $S_{INAD}$<-90 dB.

Authors applied bireciprocal lattice modified wave digital elliptic filters for this realization. Filter coefficients are designed with the authors' program prepared in the Matlab environment, based on methods presented in [2, 8]. The interpolator was realized with the ADSP-21065L digital signal processor. The interpolator structure is depicted in Fig. 5. The resulting value of the coefficient $\gamma_{sw1}$ is described by the following equation

$$\gamma_{sw1} = \gamma_{s12}\gamma_{s22}\gamma_{s32} \quad , \tag{2}$$

where: $\gamma_{s12}$, $\gamma_{s22}$, $\gamma_{s32}$ are the resultant coefficients of the upper branches for stages 1, 2, and 3, respectively. Other coefficients $\gamma_{sw2}...\gamma_{sw8}$ can be similarly calculated. Frequency response of the cascaded interpolator realized with the ADSP21061 digital signal processor for $R$=8 is shown in Fig. 6. The designed interpolator achieves the signal-to-noise and distortion ratio $S_{INAD}$ near to –90 dB and the passband ripple $\delta_p \approx 8 \cdot 10^{-9}$ dB. To compute the response for a single input sample the program needs 50 multiplications and 42 additions [8].

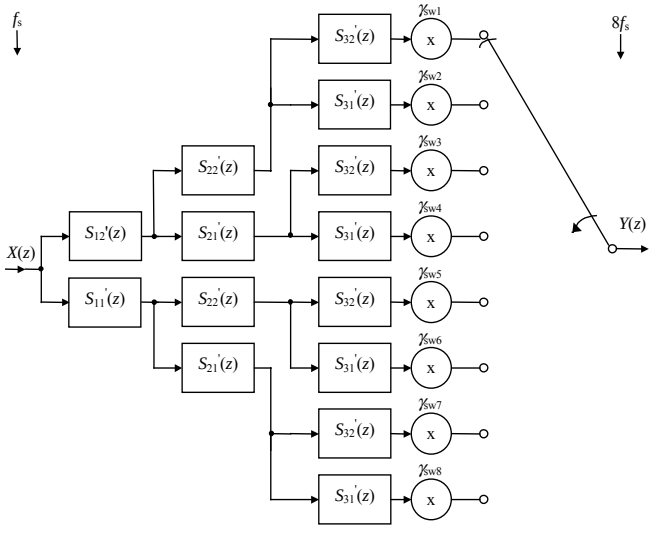


Fig. 5. Block diagram of the cascaded version of the interpolator with a single switch and resultant multipliers

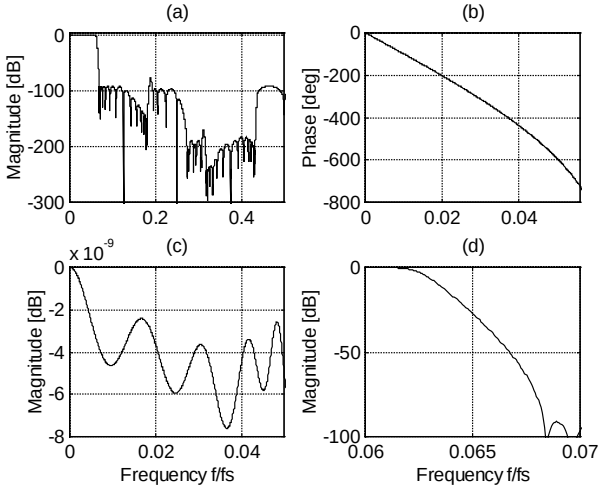


Fig. 6. Frequency response of cascaded interpolator realized with ADSP-21065L for $R$=8: (a), (c), (d) magnitude response, (b) phase response

*Digital-to-time converter with Noise Shaping*

Different circuit architectures can be used for spectral shaping of the quantization noise, i.e. for moving it away from the band of interest towards higher frequencies [1]. Block diagram of the circuit using a linear quantizer model with noise shaping is shown in Fig. 7. Output signal can be calculated as

$$Y_q(z) = X(z) - \overbrace{(1-H(z))}^{H_n(z)}E(z) = \\ = X(z)H_s(z) + E(z)H_n(z) \; . \tag{3}$$

A properly designed circuit with noise shaping has flat frequency response $H_s(\omega)$ in the signal frequency. On the other hand, $H_n(\omega)$ should have high attenuation in the frequency band of interest and a low attenuation in the rest of the band. For a low oversampling ratio $R$, an efficient way to increase the signal-to-noise ratio is the use of a second-order loop filter.

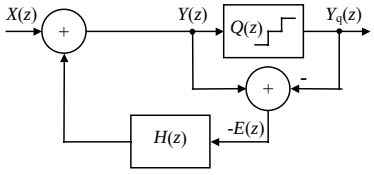


Fig. 7. Block diagram of circuit with noise shaping

Its $z$-domain output can be expressed as a sum of the signal and the quantization noise components by using a linear quantizer model

$$Y_q(z) = X(z) + (1-z^{-1})^2 E(z) \; . \tag{4}$$

The noise shaping is described by the expression that shapes the noise spectrum $E(z)$. For oversampling ratio $R$=8 and the second order noise-shaping circuit, the achieved noise suppression factor is near 23 dB.

A concept of a D/A converter with the D/A conversion error compensation [3, 11] can be combined with the idea of the PWM D/A converter based on the second order noise shaping circuit as depicted in Fig. 7.

$$Y_q(z)=\begin{cases}0 & \text{for } \left|N_p/2\,Y(z)\right|-Y_{qm}<Y_{q(min)}\\ N_p/2-Y_{qm} & \text{for } N_p/2\,Y(z)-Y_{qm}>N_p/2\\ -N_p/2-Y_{qm} & \text{for } N_p/2\,Y(z)+Y_{qm}<-N_p/2\\ \text{int}\left(N_p/2\,Y(z)\right)-Y_{qm} & \text{for other } Y(z)\end{cases}, \tag{5}$$

where:

$Y_{qm}$ — represents the transistor dead time,

$Y_{q(min)}$ — represents the transistor minimum switch on time.

The signal $Y(z)$ is transformed into signals $G_1$, $G_2$, $G_3$, and $G_4$ controlling the power pulse amplifier MOSFET transistors. High levels of these signals switch on the respective transistors. When signal $G_{1H}$ is in the high sate, the period $t_{1H}$ is calculated using (5) and period $t_{1L}$ is calculated using a similar equation for signal $G_{1L}$ in the high state.

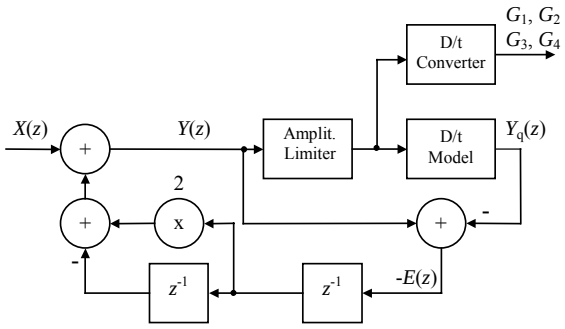


Fig. 8. Block diagram of noise shaping modulator

*C. Pulse amplifier*

Simplified model of the power pulse amplifier with LC output filter is shown in Fig. 3.

The transfer function of the simplified model (Fig. 9) is described by equation

$$y = D_{in}u_s\ , \tag{6}$$

where:

$u_s$ - represents the supply voltage,

$y$ — represents the output voltage,

$D_{in}$ — is the input duty ratio.

The supply voltage ripple is transformed to the output signal. For high quality applications, a high performance supplier and/or a special ripple compensation circuit are needed [3, 11, 10, 9, 8, 7]. In the proposed solution a high quality pulse supplier was used. The block diagram of applied solutions is presented in Fig. 10.

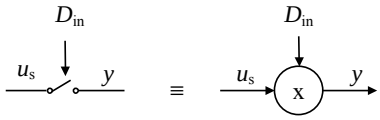


Fig. 9. Simplified model of power pulse amplifier

The output signal volume is controlled by changing pulse amplifier supply $U_s$ voltage. The pulse supplier output voltage $U_s$ is controlled by signal $w(nT)$ and by D/A converter.

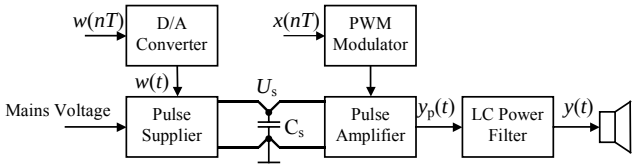


Fig. 10. Simplified block diagram of supply circuit for pulse amplifier

Another solution of such a compensation circuit for the continuous time input signal can be a one-cycle control circuit proposed by Smedley [10]. The continuous-time signal used by a one-cycle controller is not convenient for the digital signal source. For this purpose an analogue compensation circuit is proposed by the authors. Simplified diagram of this compensation circuit is shown in Fig. 11. The circuit consists two sets of integrators, comparators and switches. In every one set integrated input signal $D_{in}(n)$ and second one controlled power transistors. Input signal is a square wave with duty ratio $D_{in}(n)$ and the output signal is a square wave with duty ratio $D_{out}(n)$. For all components constant during the switching period $T_p$, it is possible to calculate $D_{out}(n)$ from equation

$$D_{out}(n)=\frac{U_{ref\,2}}{U_{p1P}(n)}D_{in}(n)-(1-D_{in}(n))\frac{U_{ref\,1}}{U_{p1P}(n)} +(1-D_{out}(n-1))\frac{U_{p1N}(n-1)}{U_{p1P}(n)}\ , \tag{7}$$

where:

$U_{ref1}$, $U_{ref2}$ - reference voltages,

$U_{p1P}$ - output voltage when transistor $Q_1$ is switched on,

$U_{p1N}$ - output voltage when transistor $Q_2$ is switched on.

A simplified small signal model of the compensation circuit and its ripple rejections for different duty ratios $D_{in}$ are shown in Fig. 12. Its small signal transfer function is

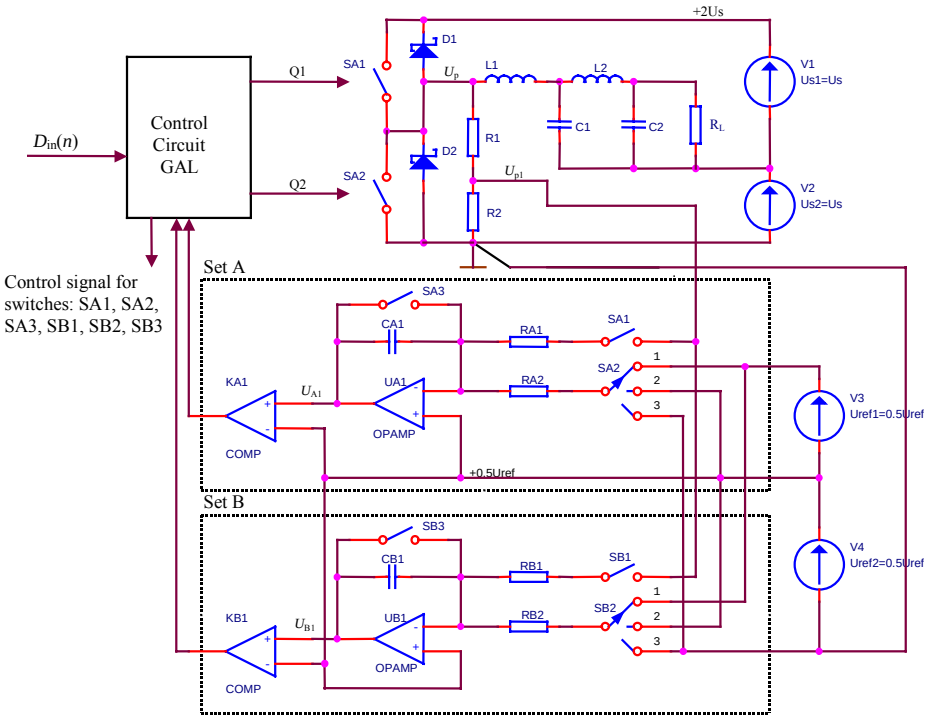


Fig. 11. Simplified diagram of analogue compensation circuit

$$y = xD_{\text{in}}\left(\frac{\tau s}{1+\tau s}\right) \quad , \qquad (8)$$

where: $\tau$- integrator time constant.

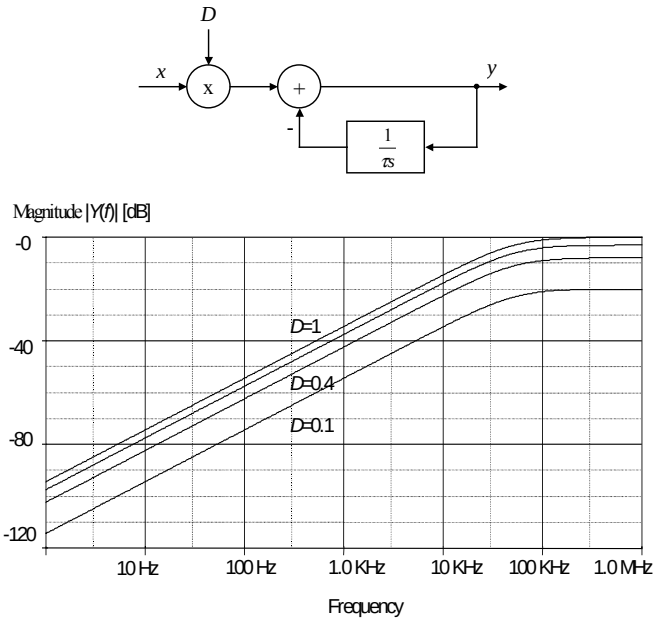


Fig.12. Small signal model of compensation circuit and its ripple rejections for different duty ratios *D*

### *D. Digital System Realization Scheme*

The filter bank, interpolator and noise shaping circuit are realized with the digital signal processor ADSP-21065. The digital PWM is realized with HCMOS counters and it has an 8-bit resolution. The counters work with frequency $f_r$=90.3168 MHz. The digital input signal from CD player has a 16-bit resolution, but processor calculations are made using the 40-bit internal floating point format. The digital PWM is controlled by 8-bit words from the digital signal processor. The realization scheme of the digital speaker system is depicted in Fig. 13 [11].

## III. ACHIEVED RESULTS

The described pulse power amplifier controlled by the hybrid PWM modulator achieves the signal-to-noise ratio (SNR) near to 75 dB in the audio band (20 Hz to 20 kHz). The output signal spectrum for this band measured with a sinusoidal input signal with frequency $f$=15 kHz is shown in Fig. 14.

## IV. CONCLUSIONS

The described digital speaker system is characterized by a simpler signal path scheme (i.e., the path from the digital signal source to the analog output — the speakers) than its classical (passive) counterpart (Fig. 1a).

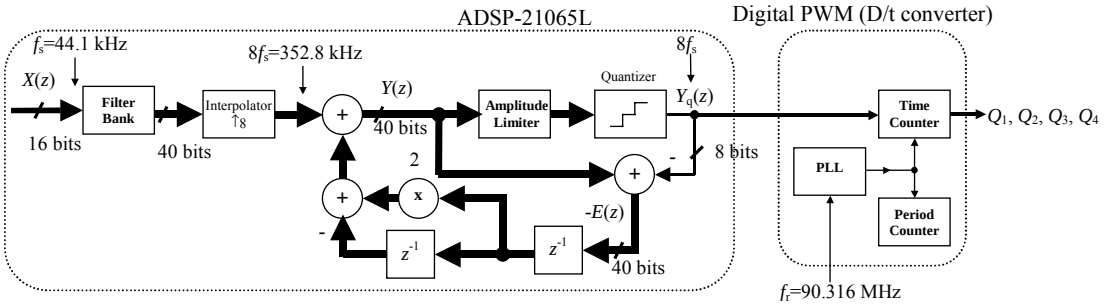


Fig. 13. Block diagram for the realization of the proposed digital speaker system

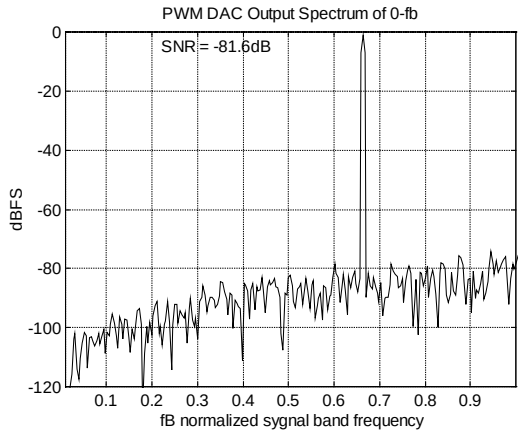


Fig. 14. Output spectrum of pulse power amplifier controlled by hybrid PWM modulator for a sinusoidal input signal with $f$=15 kHz

The digital system, implemented with a digital signal processor, directly controls the power pulse amplifier using a digital-to-time converter with noise shaping. Unlike the other so-called digital amplifiers, no analog feedback or analog signal processing amplification is involved at any stage of the presented system. The resulting system is thus a high power DAC device that translates the digital information directly into sound.

The presented concept is characterized by numerous advantages:

- signal distortion is totally coherent with the sound (music), no ringing or decay effects can appear,
- transient intermodulation cannot occur,
- distortion is the same under steady state and dynamic conditions.

In the further research, the noise shaping circuit will be developed to achieve better noise rejection. In near future digital PWM circuit will be realized with CLPD circuit with 9-bit resolution and working frequency $f_r$=180.6336 MHz.

In the authors' opinion, in the near future, directly digitally driven class-D power amplifiers will be more and more popular, especially for high power and/or high quality audio applications.

Presented circuits and methods are useful not only for audio applications, authors are using this technique for other power electronics applications such as: active power filter, power conditioners, high quality AC sources etc.

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