Implementation of Modified Wave Digital Filters Using Digital Signal Processors

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ABSTRACT

This paper describes implementation of multirate modified lattice wave digital filters using digital signal processors. Cascaded interpolator based on bireciprocal modified lattice wave digital filters for interpolating of high quality audio signals is presented. The interpolator is implemented in ADSP-21065L digital signal processor. The methodology for this and the results are presented. The frequency response of the cascaded interpolator realized with the ADSP-21065L processor is analyzed for interpolation ratio R=8. This interpolator achieves the signal-to-noise and distortion ratio S_{INAD} *near to 90dB and the passband ripple of* $\delta_p \approx 8\cdot 10^{-6}$ *dB.*

1. INTRODUCTION

Wave digital filters (WDF's) are known to have many advantageous properties [4]. They have a relatively low passband sensitivity to coefficients, small rounding errors, big resistivity to parasitic oscillations (limit cycles), great dynamic range, low level of the rounding noise, etc. Especially favorable are the lattice wave digital filters. They are well suited for the high quality audio signal processing.

Lattice wave digital filters are built with two blocks realizing all-pass functions S_1(z) and S_2(z). Typically blocks S_1(z) and S_2(z) are realized by a cascade of first-order and second-order all-pass sections. The transfer function of a lattice WDF can be written as

$$H(z) = 0.5\left(S_1(z) + S_2(z)\right) \quad . \tag{1}$$

These allpass filters can be realized in several ways described in [4]. One approach that yields parallel and modular filter algorithms is the use of cascaded first and second-order sections. The first and the second-order all-pass sections are here realized using symmetric two-port adaptors. Typical classical two-port adaptors are depicted in Fig. 2. Reflection signals b_1 and b_2 can be calculated by equations

$$\begin{cases} b_1 = -\gamma_1 a_1 + (1+\gamma_1) a_2 \\ b_2 = (1-\gamma_1) a_1 + \gamma_1 a_2 \quad . \end{cases} \tag{2}$$

Both classic first-order all-pass sections shown in Fig. 2b, c require a single multiplication and three additions. These two versions have, however, different lengths of critical paths. The critical path of the all-pass section in Fig. 2b consists of a single multiplier and two summers, while that in Fig. 2c —of a single multiplier and three summers. The first version is better for the implementation in a digital signal processor with a parallel instruction set.

Wave digital filters were proposed by Fettweis in 70's, i.e., when multiplication was an expensive operation. That is why they were originally designed to minimize the number of multipliers. It is still advantageous, if the filter is implemented in a simple digital hardware structure (FPGA, ASIC, etc.) but can be undesirable for realizations with modern digital signal processors (DSP's). In typical DSP's a single computing cycle consists of a multiplication combined with accumulation and to/from memory data moving operations. In result, an individual addition also requires one computing cycle. This is a disadvantage for implementing WDF's by modern digital signal processors, especially with floating point arithmetic.

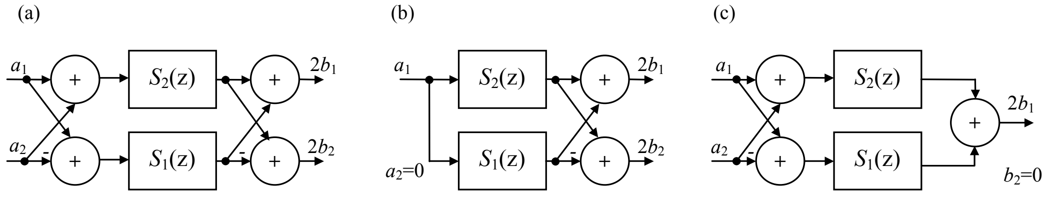


Fig. 1. Simplified block diagrams of lattice wave digital filters: (a), (b) analysis filter bank, (c) synthesis filter bank

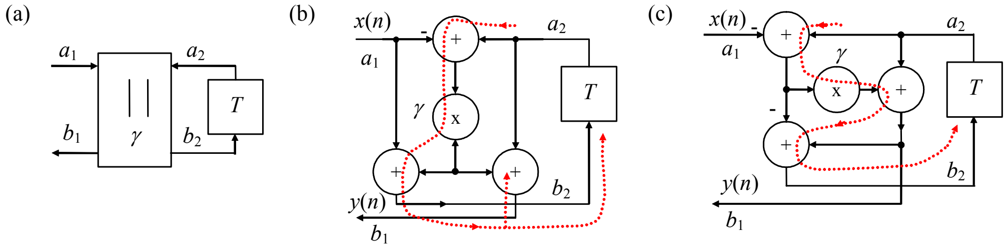


Fig. 2. First-order all-pass sections: (a) block diagram of a classic section, (b), (c) two realizations of a two-port adaptor

2. MODIFIED WAVE DIGITAL FILTERS

Today, modern digital signal processors are designed to be able to calculate multiplication together with addition (or more) in a single operational cycle. In result the classical two-port adaptor structure of Fig. 2b is ineffective for the DSP realization, especially for the floating point arithmetic. That is why modified structures have been proposed. The idea of modified wave digital filters, i.e., those with equal numbers of additions and multiplications and with short critical paths were proposed by Fettweis in [5]. In Figure 3 this idea consisting in inclusion of two additional complementary multipliers is illustrated.

Reflection signals $b_1^{'}$ and b_2 of the modified two-port adaptor (Fig. 4a) can be calculated by equations

$$\begin{cases} b_1^{'} = \gamma_{11}a_1^{'} + \gamma_{12}a_2 \\ b_2 = \gamma_{21}a_1^{'} + \gamma_{22}a_2 \end{cases} , \tag{3}$$

in which coefficients γ_{ij} are given by equations

$$\begin{cases} \gamma_{11} = -\gamma_1 \dfrac{k_{w1}}{k_{d1}} \\ \gamma_{12} = (1+\gamma_1)/k_{d1} \\ \gamma_{21} = (1-\gamma_1)k_{w1} \\ \gamma_{22} = \gamma_1 \end{cases} . \tag{4}$$

Three cases for the realization of modified two-port adaptors are possible. They are described by equations listed in Table 1 and depicted in Figs. 4b, 4c and 4d.

Every realization needs four operations: two multiplications and two additions. In cases 1 and 3, the critical path consists of only two arithmetic operations.

As an example, the realization an N-order branch of the lattice filter with modified first-order sections is depicted in Fig. 5. The resulting value of the overall branch coefficient can be calculated as

$$\gamma_s = \prod_{i=1}^{N} \frac{k_{di}}{k_{wi}} . \tag{5}$$

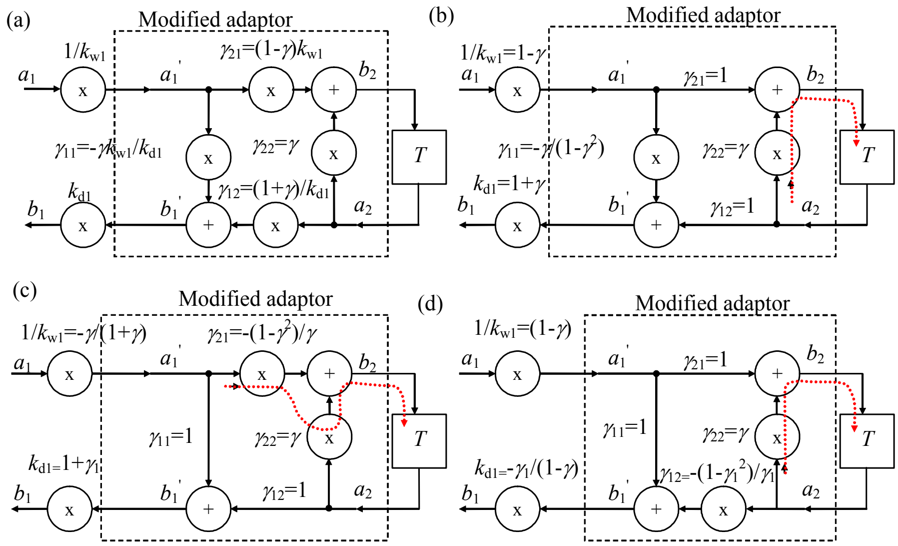


Fig. 4. Block diagrams of first-order modified all-pass sections: (a), (b) case 1, (c) case 2, (d) case 3

Table 1. Equations for the first-order modified all-pass sections

Case 1 for: $\gamma_{21}=1$, $\gamma_{12}=1$	Case 2 for: $\gamma_{11}=1$, $\gamma_{12}=1$	Case 3 for: $\gamma_{11}=1$, $\gamma_{21}=1$
$\begin{cases} k_{w1} = 1/(1-\gamma) \\ k_{d1} = 1+\gamma \end{cases}$	$\begin{cases} k_{w1} = -(1+\gamma)/\gamma \\ k_{d1} = 1+\gamma \end{cases}$	$\begin{cases} k_{w1} = 1/(1-\gamma) \\ k_{d1} = -\gamma_1/(1-\gamma) \end{cases}$
$\begin{cases} \gamma_{11} = -\gamma/(1-\gamma^2) \\ \gamma_{12} = 1 \\ \gamma_{21} = 1 \\ \gamma_{22} = \gamma \end{cases}$	$\begin{cases} \gamma_{11} = 1 \\ \gamma_{12} = 1 \\ \gamma_{21} = -(1-\gamma^2)/\gamma \\ \gamma_{22} = \gamma \end{cases}$	$\begin{cases} \gamma_{11} = 1 \\ \gamma_{12} = -(1-\gamma^2)/\gamma \\ \gamma_{21} = 1 \\ \gamma_{22} = \gamma \end{cases}$

Author realization of the modified first-order section with the ADSP-21065L digital signal processor is presented in Fig. 6.

3. INTERPOLATOR

A special class of lattice wave digital filters referred to as bireciprocal, is suitable for the realization of interpolators. Characteristic function $K(\psi)$ of bireciprocal filters satisfies equation

$$K(\psi) = \frac{1}{K\left(\frac{1}{\psi}\right)} \quad , \quad \text{where} \quad \psi = \frac{z-1}{z+1} \quad . \tag{6}$$

For this kind of filters every even filter coefficient is equal to zero and the filter circuit is simplified.

Bireciprocal lattice wave digital filters of this kind are very useful for building interpolators. A cascaded version of such an interpolator with bireciprocal modified lattice wave digital filters is shown in Fig. 7a. The filter first-order modified all-pass sections are realized as in Fig. 6.

As an illustrative example a cascaded interpolator for a class-D power audio amplifier [3, 6] is used. Parameters chosen by the authors for this interpolator are: passband ripple $\delta_p < 0.1$ dB, oversampling ratio R=8, passband 4...20 kHz, signal-to-noise and distortion ratio $S_{INAD} < 90$ dB. Authors applied bireciprocal lattice wave digital elliptic filters for this realization. Filter coefficients are designed with authors' program prepared in the Matlab environment, based on the methods presented in [6].

The interpolator was realized with ADSP-21065L signal processor by Texas Instruments using modified wave digital filters. The structure of the interpolator is depicted in Fig. 7b. The resulting value of the coefficient γ_{sw1} is given by the following equation

$$\gamma_{sw1} = \gamma_{s12}\gamma_{s22}\gamma_{s32} \quad , \tag{7}$$

where: γ_{s12}, γ_{s22}, γ_{s32} are the resultant coefficients of upper branches for stages 1, 2, 3, respectively.

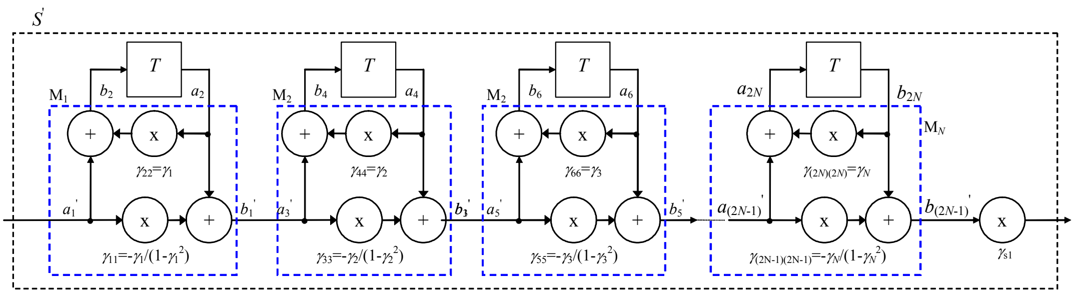
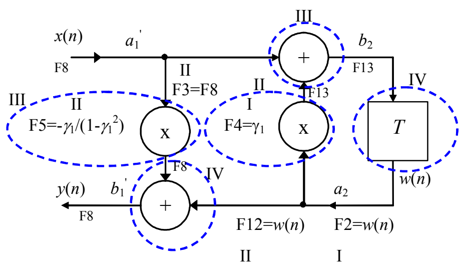


Fig. 5. Diagram of the N-order branch of the lattice wave digital filter realized by first-order sections

(a)



(b)

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Initialization: input sample x(n) in register F8:
    B0=address_w; L0=0; M0=1, M1=0;     { address w(n) →B0 }
    B8=address_g; L8=0; M8=1;           { address γ1 →B8, address -γ1/(1-γ1²) →B8+1, }

I.   Clear F12, get from memory: F2=w(n), F4=γ1
         F12=F12-F12, F2=dm(I0,M0), F4=pm(I8,M8);
II.  Calculate: F13= γ1·w(n), move x(n) do F3, get from memory-γ1(1-γ1²) do F5 i w(n) do F12:
         F13=F2*F4, F3=F8+F12, F12=dm(I0,M0), F5=pm(I8,M8);
III. Calculate:F8=-γ1(1-γ1²) x(n), F13=w(n+1)=x(n) + γ1·w(n), F2=x(n)
         F8=F3*F5, F13=F8+F13;
IV.  Calculate:F8=y(n) =-w(n)-γ1(1-γ1²) x(n), save in memory w(n+1)=F13:
         F8=F8+F12, dm(I0,M0)=F13;
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Fig. 6. Realization of modified first-order all-pass section with ADSP-21065L: (a) realization diagram of the first-order section, (b) corresponding assembler program

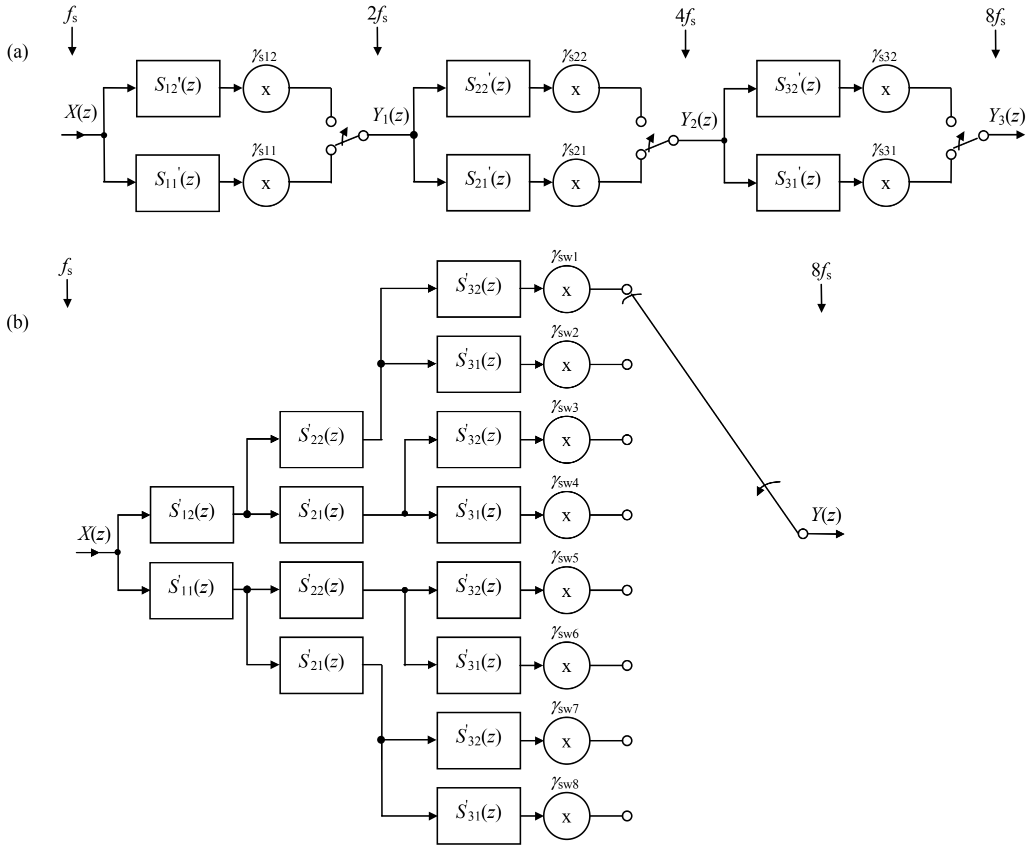

Fig. 7. Cascaded version of the interpolator for $R = 8$ (a), version of the interpolator with a single switch and the resulting multipliers (b)

Other resultant coefficients $\gamma_{sw2}...\gamma_{sw8}$ can be similarly calculated. The cascaded interpolator realized with the ADSP-21065L for R=8 achieves the signal-to-noise and distortion ratio S_{INAD} near to 90dB.

4. CONCLUSIONS

The presented modified wave digital filters are very efficient for the implementation in modern floating-point digital signal processors such as the ADSP-21065L processor and the VLIW architecture TMS320C6000 processor. They are especially important for large dynamic range applications. Similarly modified ladder wave digital filters can be designed.

5. REFERENCES

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