Digital Control Circuit for Active Power Filter with Modified Instantaneous Reactive Power Control Algorithm

Krzysztof Sozański, Ryszard Strzelecki, Adam Kempski
University of Zielona Góra, Institute of Electrical Engineering
ul. Podgórna 50, 65-246 Zielona Góra, Poland

Abstract - This paper describes the proposed active power filter with the control circuit based on the modified instantaneous reactive power control algorithm. The control circuit was realized using digital signal processor ADSP-21065. In the proposed circuit a advanced current controller algorithm realized using the digital signal processor ADSP-21065 is employed. The active power filter circuit was build and tested. Some illustrative, experimental results are also presented in the paper.

I. Introduction

Recent wide spread of power electronic equipment has caused an increase of the harmonic disturbances in the power distribution systems. The control of AC power thyristors and other semiconductor switches is widely employed to feed electric power to electrical loads, such as: furnaces, computer power supplies, adjustable speed drives etc. The nonlinear loads draw harmonic and reactive power components of current from AC mains. In three-phase systems, they could also cause unbalance and draw excessive neutral currents. Reactive power burden, injected harmonics, unbalance, and draw excessive neutral currents cause a poor power factor and a low power system efficiency.

Conventionally, passive *LC* filters and capacitors have been used to eliminate line current harmonics and to increase the power factor. However, in some practical applications, in which the amplitude and the harmonic content of the distortion power can vary randomly, this conventional solution becomes ineffective.
To suppress these harmonics, an active power-harmonic-compensation filter should be used. The active power filter (APF) can be connected in series or in parallel with the supply network. The series APF is applicable to the harmonic compensation of a large capacity diode rectifier with a DC link capacitor. The parallel APF (shunt active power filter) permits to compensate the harmonics and asymmetries of the mains currents caused by nonlinear loads. Two version of harmonic compensation circuit with current-fed active power filter is depicted in Fig. 1. In Fig. 1a is shown APF without feedback (with unity gain) and in Fig. 1b APF with feedback. According to its better stability for realization was chosen APF without feedback (Fig. 1a).

Shunt active power filter injects AC power current i_C to cancel the main AC harmonic content.

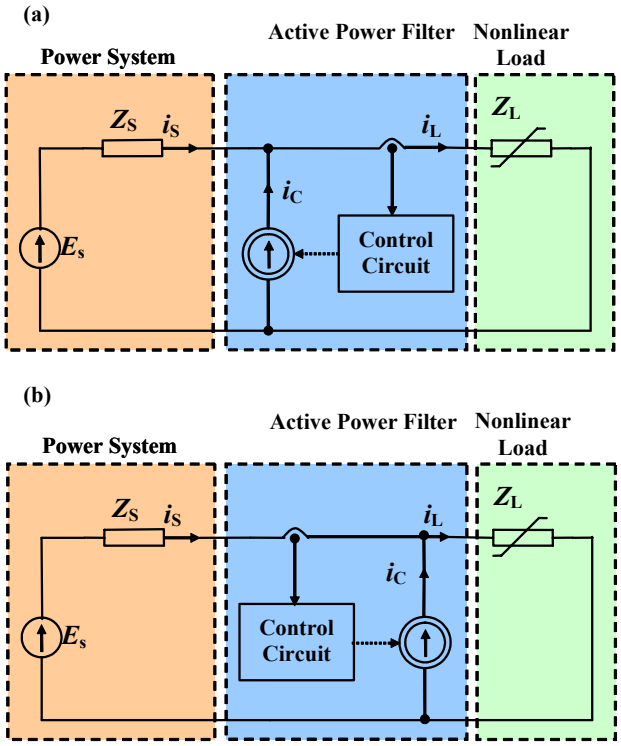

Fig. 1. Harmonic compensation circuit with current-fed active power filters: (a) without feedback (with unity gain) , (b) with feedback

The line current i_S is the result of summing the load current i_L and the compensating current i_C

$$i_S = i_L + i_{C1} + i_{C2} \ . \qquad (1)$$

II. Proposed Active Power Filter

Simplified block diagram of the proposed active power compensation circuit with the parallel APF for power of 75 kVA is depicted in Fig. 2. The circuit consists of the power part with a three-phase IGBT power transistor bridge IPM (intelligent power module) connected to the AC mains through an inductive filtering system composed of inductors L_1, L_2, L_3. The APF circuit contains a DC energy storage, ensured by two capacitors C_1 and C_2. The control circuit is realized using the digital signal processor ADSP-21065. The active power filter injects the harmonic currents I_{C1}, I_{C2}, I_{C3} into the power network and offers a notable compensation for harmonics, reactive power and unbalance. The filter is designed for three and four wire loads.

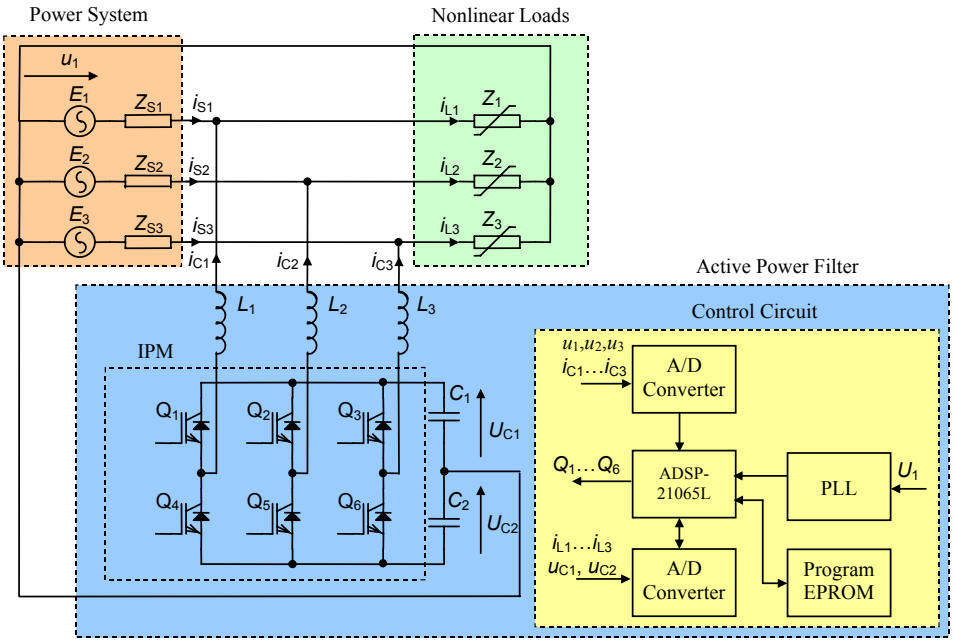

Fig. 2. Simplified block diagram of the proposed active power compensation circuit

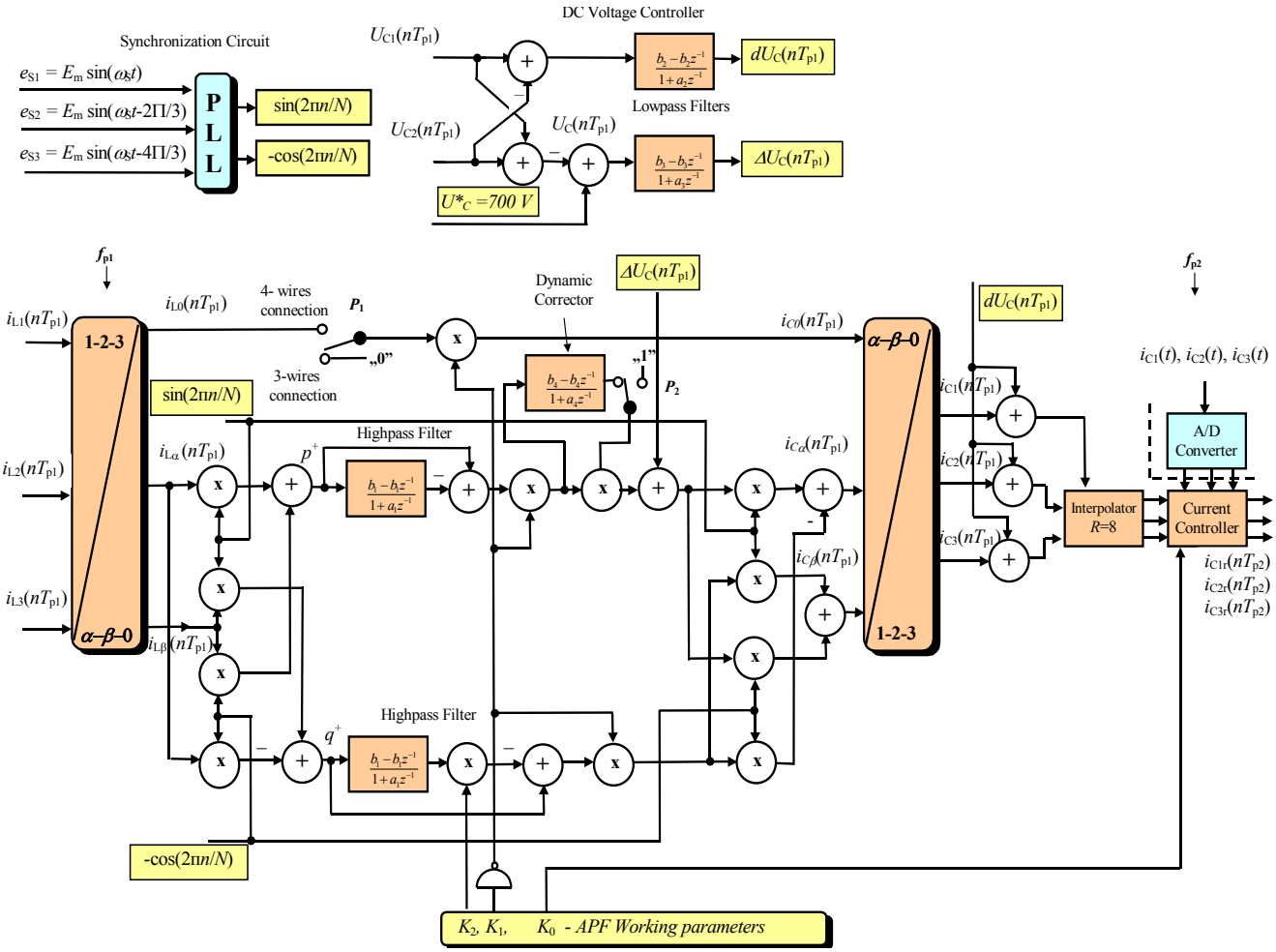

Fig. 3. Simplified block diagram for the active power filter control algorithm

A. Control algorithm

Control algorithm for the proposed APF is based on the strategy resulting from the instantaneous reactive power theory initially developed by Akagi *et al.* [1]. Simplified block diagram for the active power filter control algorithm is depicted in Fig. 3. (based on the circuit designed in [3, 6]). To the classical instantaneous reactive power algorithm are added additional control parameters, they are described in Table 1.

TABLE 1

APF CONTROL PARAMETERS

Name	Value of parameter
K_0	1- APF transistors are switch off, capacitors C_1 and $C2$ are charged to initial voltage 510V 0 – APF transistors are switch on
K_1	1- APF compensator is switch off, working only capacitors voltage regulator, capacitors C_1 and C_2 are charged to nominal working voltage 690V 0 - APF compensator is switch on
K_2	Value of parameter varying from 0 to 1 1- Harmonics and asymmetry are compensated 0 – Full compensation of reactive power
P_1	3 wire or 4-wire circuit

The algorithm realized using the digital signal processor ADSP-21065L is divided into two parts: the first one has sampling rate f_{p1} and the second has sampling rate f_{p2}. The digital signal processor is synchronized with the mains voltage U_1 and the algorithm is performed RN times per the mains period. The sampling periods can be calculated with the formula

$$T_{p1} = \frac{T_s}{N} \quad \text{and} \quad T_{p2} = \frac{T_s}{RN} \tag{2ab}$$

where:
T_s – period of the mains voltage,
$f_s = T_s^{-1}$ – frequency of the mains voltage,
R – oversampling ratio,
N – total number of samples per mains period.

For the mains voltage frequency of f_s=50 Hz and the number of samples chosen to N=256 and R=8, the sampling periods is equal T_{p1} =78.125 μs, T_{p2} =7.766 μs and the sampling rate is equal to f_{p1}=12800 samples/s f_{p2}=102400 samples/s. Three-phase current signals can be transformed into the equivalent two-phase representation. The transformation (1-2-3 → α-β-0) from the three-phase current signals $i_{L1}(nT_{p1})$, $i_{L2}(nT_{p1})$ $i_{L3}(nT_{p1})$, to the two-phase $i_{L\alpha}$, $i_{L\beta}$ with an additional neutral signal i_{L0} can be written in a matrix form as

$$\begin{bmatrix} i_{L\alpha}(nT_{p1}) \\ i_{L\beta}(nT_{p1}) \\ i_{L0}(nT_{p1}) \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{6} & 1/\sqrt{6} & 1/\sqrt{6} \end{bmatrix} \begin{bmatrix} i_{L1}(nT_{p1}) \\ i_{L2}(nT_{p1}) \\ i_{L3}(nT_{p1}) \end{bmatrix} \tag{3}$$

where: $i_{L\alpha}(nT_{p1})$ – digital representation of signal $i_{L\alpha}$ for sampling period T_{p1},
n – index of the current sample.

In the next step, the two-phase signals are transformed from the rotating to the stationary reference frame. This transformation is commonly called the reverse Park transformation and can be digitally calculated by equations

$$\begin{cases} p^+(nT_{p1}) = i_{L\alpha}(nT_{p1}) \sin\left(\frac{2\pi n}{N}\right) - i_{L\beta}(nT_{p1}) \cos\left(\frac{2\pi n}{N}\right) \\ q^+(nT_{p1}) = i_{L\alpha}(nT_{p1}) \cos\left(\frac{2\pi n}{N}\right) + i_{L\beta}(nT_{p1}) \sin\left(\frac{2\pi n}{N}\right) \end{cases} \tag{4}$$

and the digital sinusoidal reference signal is given by formula

$$\sin\left(\frac{2\pi n}{N}\right) = \sin\left(\frac{2\pi f_{p1} n T_{p1}}{N}\right) . \tag{5}$$

In order to generate the reference sinusoidal and cosinusoidal signals, a table containing sinus function values is allocated in the digital signal processor program memory. Signal $p^+(nT_{p1})$ represents instantaneous active power and signal $q^+(nT_{p1})$ instantaneous reactive power. The DC components of signals $p^+(nT_{p1})$ and $q^+(nT_{p1})$ are removed by a high-pass digital IIR filter. The low pas filter is described by equation

$$H(z) = \frac{b - bz^{-1}}{1 + az^{-1}} ,$$

and

$$b = \frac{2\frac{T_1}{T_{p1}}}{1 + 2\frac{T_1}{T_{p1}}} , \quad a = \frac{1 - 2\frac{T_1}{T_{p1}}}{1 + 2\frac{T_1}{T_{p1}}} \tag{6abc}$$

where: T_1 – the reference (analog) filter time constant.

For stabilizing the DC voltage a proportional controller is used, response of it is calculated by equation

$$\Delta U_{C12}(nT_{p1}) = k_P \left(U_R(nT_{p1}) - \left(U_{C1}(nT_{p1}) + U_{C2}(nT_{p1}) \right) \right) \tag{7}$$

where:
U_{C1}, U_{C2} – voltage on capacitor C_1 and C_2, respectively,
k_P – gain of voltage controller,
U_R – DC reference voltage.

Signal $\Delta U_{C12}(nT_{p1})$ is subtracted from the component $p^+(nT_{p1})$

$$p_C^+(nT_{p1}) = p^+(nT_{p1}) - \Delta U_{C12}(nT_{p1}) . \tag{8}$$

In the next step components p_C^+ and q^+ are transformed by Park transformation to the two-phase representation

$$\begin{cases} i_{\mathrm{CR}\,\alpha}(nT_{p1}) = p_{\mathrm{C}}^{+}(nT_{p1})\sin\left(\dfrac{2\pi n}{N}\right) + q^{+}(nT_{p1})\cos\left(\dfrac{2\pi n}{N}\right) \\ i_{\mathrm{CR}\,\beta}(nT_{p1}) = -\,p_{\mathrm{C}}^{+}(nT_{p1})\cos\left(\dfrac{2\pi n}{N}\right) + q^{+}(nT_{p1})\sin\left(\dfrac{2\pi n}{N}\right) \end{cases} \tag{9}$$

and then transformed back to the three-phase reference current signals

$$\begin{bmatrix} i_{\mathrm{CR}\,1}(nT_{\mathrm{p1}}) \\ i_{\mathrm{CR}\,2}(nT_{\mathrm{p1}}) \\ i_{\mathrm{CR}\,3}(nT_{\mathrm{p1}}) \end{bmatrix} = \sqrt{\frac{3}{2}} \begin{bmatrix} 2/3 & 0 & \sqrt{6}/3 \\ -1/3 & \sqrt{3}/3 & \sqrt{6}/3 \\ -1/3 & -\sqrt{3}/3 & \sqrt{6}/3 \end{bmatrix} \begin{bmatrix} i_{\mathrm{CR}\,\alpha}(nT_{\mathrm{p1}}) \\ i_{\mathrm{CR}\,\beta}(nT_{\mathrm{p1}}) \\ i_{\mathrm{L}\,0}(nT_{\mathrm{p1}}) \end{bmatrix} \tag{10}$$

In the next step the output compensation reference current signals $i_{\mathrm{CR1}}(nT_{\mathrm{p1}})$, $i_{\mathrm{CR2}}(nT_{\mathrm{p1}})$ $i_{\mathrm{CR3}}(nT_{\mathrm{p1}})$ are interpolated with oversampling ratio R=8, to signals $i_{\mathrm{CR1}}(nT_{\mathrm{p2}})$, $i_{\mathrm{CR2}}(nT_{\mathrm{p2}})$ $i_{\mathrm{CR3}}(nT_{\mathrm{p2}})$. Block diagram of the chosen polyphase interpolator based on FIR filter with periodically time-varying coefficients is depicted in Fig. 4.

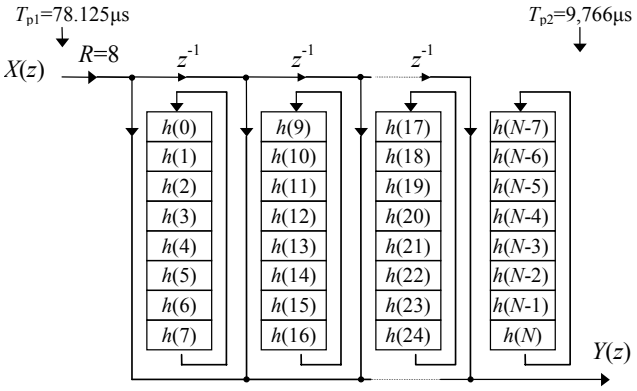

Fig. 4. Polyphase interpolator with periodically time-varying coefficients for R=8 block diagram

Finally, the output compensation reference current signals and transformed to transistor controlling pulses by current controller. Initially in the proposed circuit a hysteresis current controller algorithm realized using the digital signal processor ADSP-21065 is employed. Hysteresis control algorithm is based on a nonlinear feedback loop with two-level hysteresis comparators. The inverter switching speed depends largely on the load parameters. In the proposed APF advanced hysteresis current controller with variable width of the hysteresis (Fig. 5) is applied. It has additional improvements:

- maximum switching speed is limited,
- switching speed dependends on the 'speed history',
- switching speed is dependent on the compensation reference current signals i_{CR1}; the higher the signal level the lower is the switching speed.

Fig. 6 shows dependence of compensation reference current signals $i_{\mathrm{CR1}}(nT_{\mathrm{p2}})$ level on the switching speed. For low level the signal switching speed is around 25 kHz, and for higher level of signal is around 7 kHz.

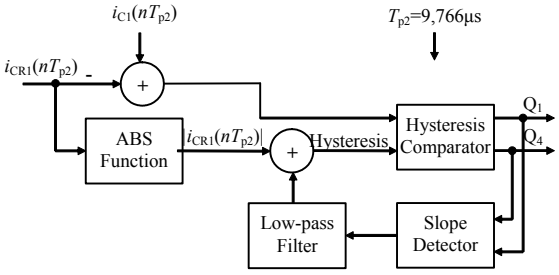

Fig. 5. Block diagram of hysteresis current controller algorithm with variable width of the hysteresis

In the next step of developing current controller algorithm, current delta sigma modulator (CDSM) [4] will be implemented.

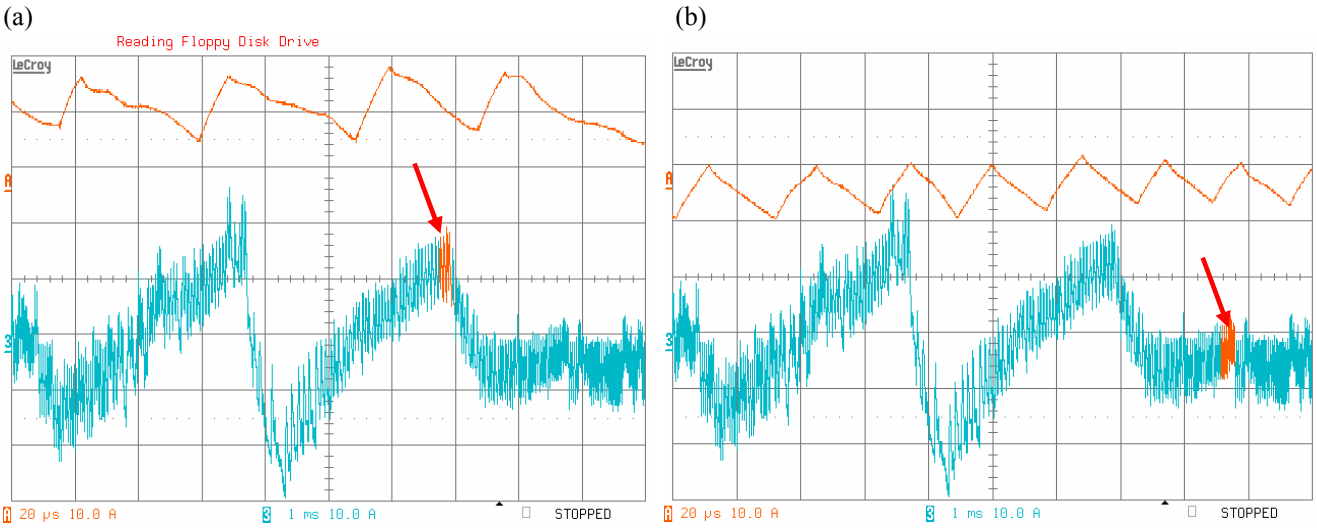

Fig. 6. Experimental waveforms, illustration of the dependence of compensation reference current signals $i_{\mathrm{CR1}}(nT_{\mathrm{p2}})$ level on the switching speed: (a) for high level of signal, (b) for low level of signal

III. ACHIEVED RESULTS

Prototype of the three-phase active power filter was build and tested in the laboratory (Fig.11). Simplified diagram of the test circuit is depicted in Fig. 8. To model the nonlinear load a thyristor power controller with the resistive and inductive loads was used. Oscillogram records of the various waveforms of the test circuit are shown in Figs. 9, 10. Fig. 9 shows the steady-state performance of the active power filter with the resistive load. There are depicted: load current I_{L1}, compensating current I_{C1}, line current I_{S1}, and supply voltage U_1 (Fig. 9a). The harmonic spectrum of the line current I_{S1} and spectrum of the load current I_{L1} is depicted in Fig. 9b. Fig. 10 shows the steady-state performance of the active power filter with the inductive load. There are depicted: load current I_{L1} and line current I_{S1}(Fig. 9a). The harmonic spectrum of the line current I_{S1} and spectrum of the load current I_{L1} is depicted in Fig. 10b.

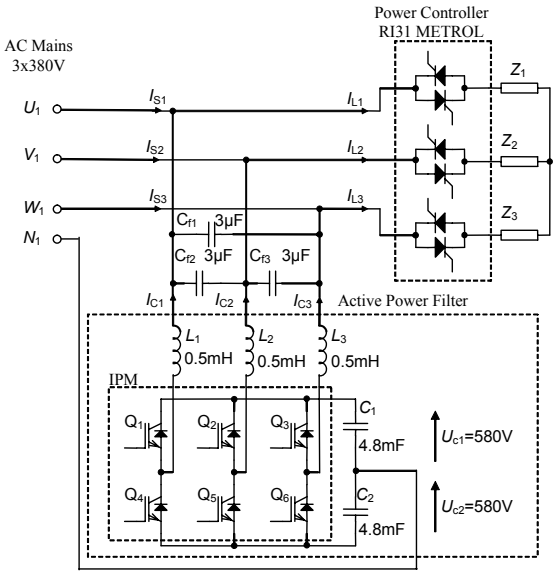

Fig. 8. Three-phase active power filter test circuit

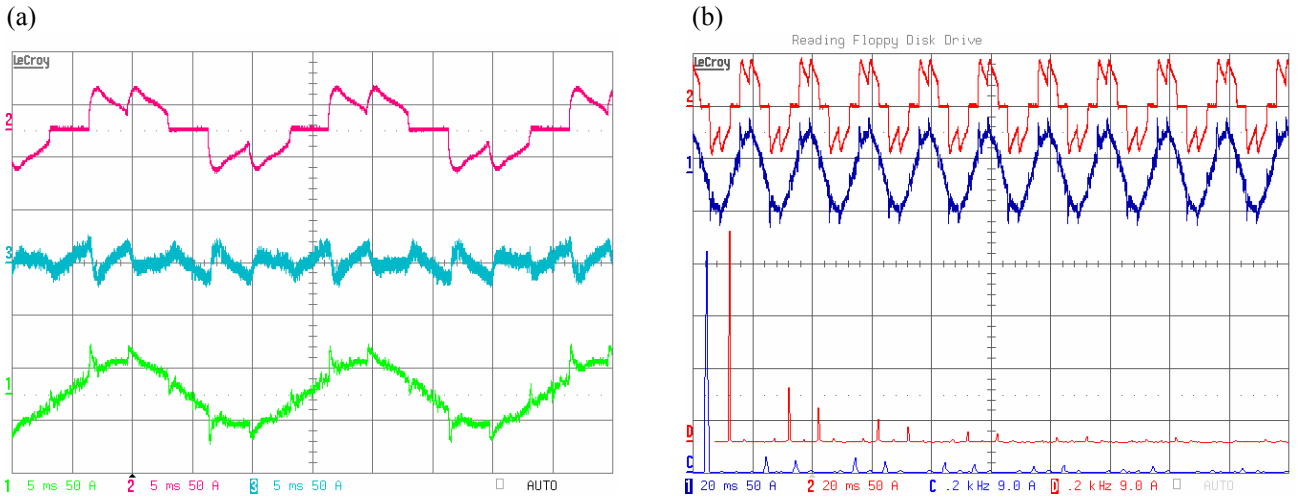

Fig. 9. Experimental waveforms of active power filter in steady-state with the resistive load: (a) curve 1 line current I_{S1} (green), curve 2 load current I_{L1} (red), curve 3 compensating current I_{C1} (blue), (b) curve 1 1oad current I_{L1} (red), curve 2 line current I_{S1} (blue), curve D harmonic spectrum of 1oad current I_{L1} (red), curve C harmonic spectrum of line current I_{S1} (blue)

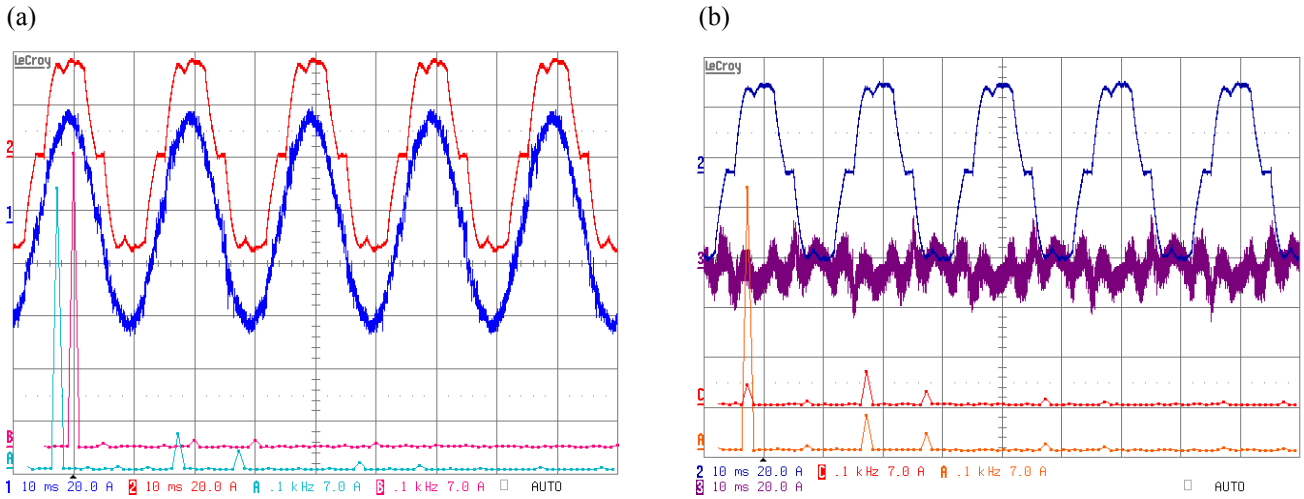

Fig. 10. Experimental waveforms of active power filter in steady-state with inductive load: (a) curve 2 1oad current I_{L1} (red), curve 2 line current I_{S1} (blue), curve A harmonic spectrum of 1oad current I_{L1} (red), curve B harmonic spectrum of line current I_{S1} (blue), (b) curve 2 1oad current I_{L1} (blue), curve 2 compensating current I_{C1} (red), curve A harmonic spectrum of 1oad current I_{L1} (red), curve C harmonic spectrum of compensating current I_{C1} (blue)

Fig. 11 Active power filter in our laboratory

IV. Conclusions

This paper describes the proposed active power filter with the control circuit based on the ADSP-21065 DSP EZ Lite Starter Kit. The new active power filter for power of 75 kVA was build and tested. Some illustrative, experimental results are also presented in the paper. The proposed technique makes the compensation process instantaneous. Control algorithm of the proposed APF based on the control strategy following from the modified instantaneous reactive power theory is implemented in the floating-point digital signal processor ADSP-21065. In the present time designed active power filter is still under development in our laboratory.

References

1. H. Akagi , Y. Kanazawa, A. Nabae, “Instantaneous Reactive Power Compensators Comprising Switching Devices without Energy Storage Components,” IEEE Transactions on Industry Applications , Vol. IA-20 N0 3, May-June 1984, pp. 625-630
2. H. Fujita, H. Akagi, “A Practical Approach To Harmonic Compensation In Power Systems,” IEEE IAS Annual Meeting Conf. Rec., 1990.
3. R. Strzelecki, R. Supronowicz, „Filtracja harmonicznych w sieciach zasilających prądu przemiennego,” Wydawnictwo Adam Marszałek, Toruń, 1998 (in Polish).
4. M. Kazimierkowski, L. Malesani, “Current Control Techniques for Three-Phase Voltage-Source Converters: A Survey,” IEEE Transactions on Industrial Electronics Vol.45 N0 5, October 1998
5. L. Malesani, L Rosseto, P. Tenti, “Active Power Filter With Hybrid Energy Storage,” IEEE Transactions on Power Electronics Vol.6 N 0 3, July 1991
6. K. Sozański, R. Strzelecki, ”Aplikacyjny układ sterowania filtrem hybrydowym z zastosowaniem procesora sygnałowego”, Sterowanie w Energoelektronice i Napędzie Elektrycznym, Politechnika Łódzka, Łódź, 1995 (in Polish).